


LCFC Confidential

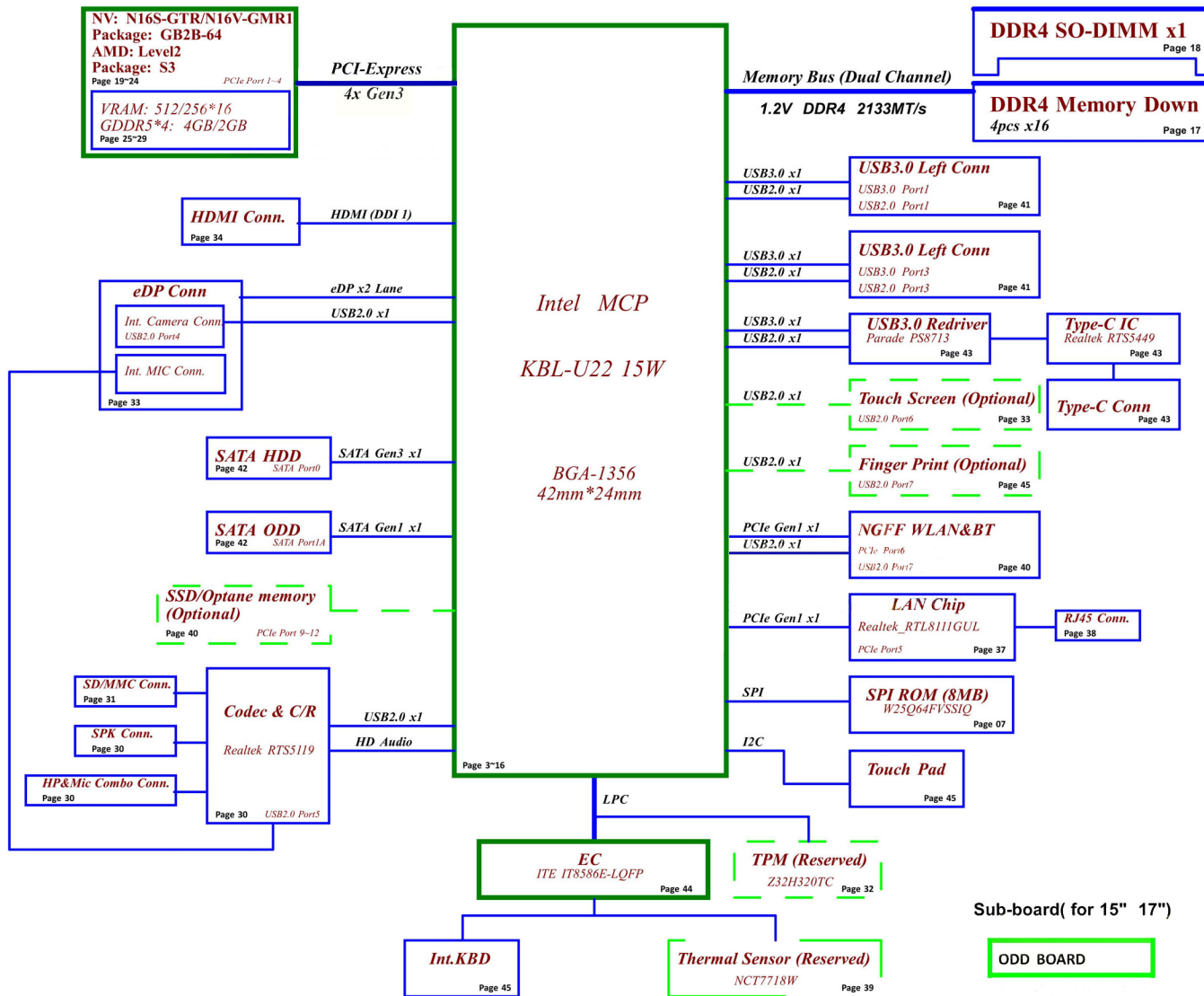
DG421/DG521/DG721 MB Schematics Document

Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2017-01-18

REV:1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page		
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Custom	DG421		1.0			
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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4 AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WINAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			Wlan	Reserved
		DGPU	need to update				

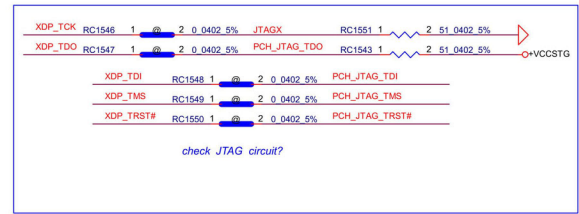
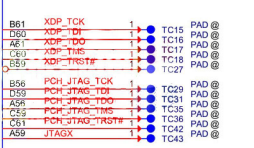
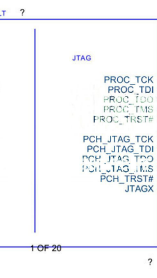
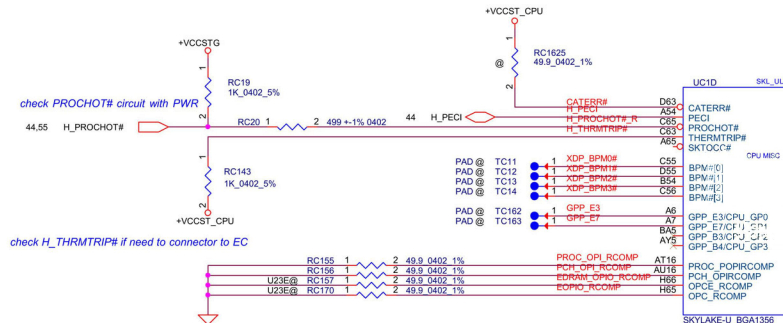
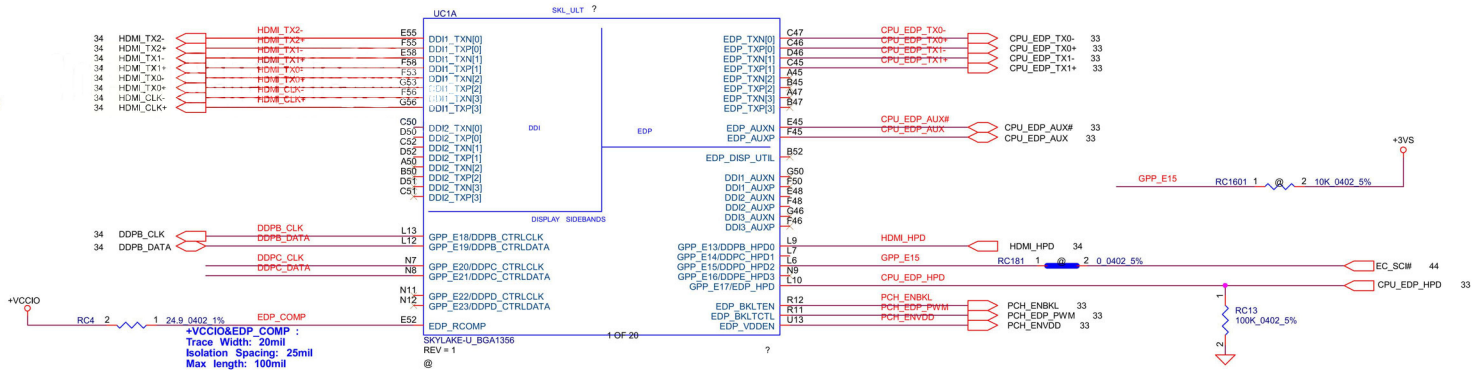
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1~4 X4 PCIE
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9~12 X4 PCIE
	Optane Memory
	0 HDD
SATA	1A ODD
	1B used as PCIE
	2 used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAM rank part
DUALRANK@	For dual VRAM rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

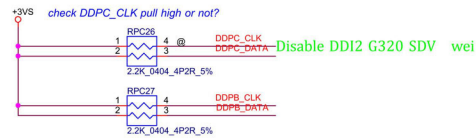
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK



DDP_CTRLDATA strapping sampled on the rising edge of PWROK

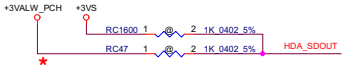
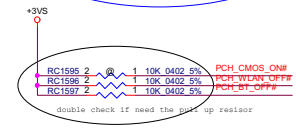
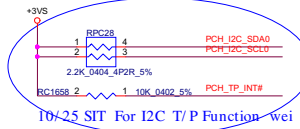
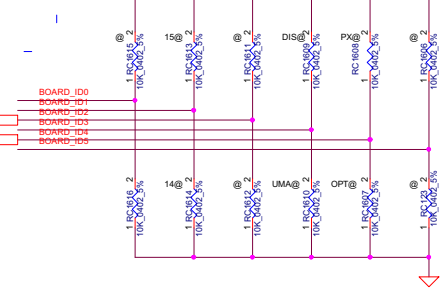
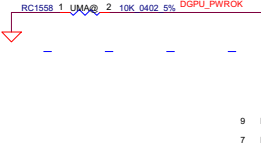
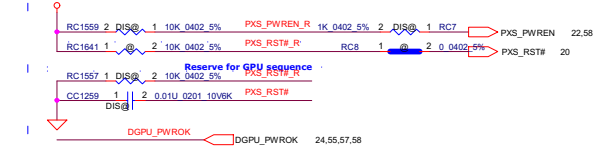
Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



@DIS For NV and AMD GPU SKU

@OPT&GC6 Only for NV GPU SKU

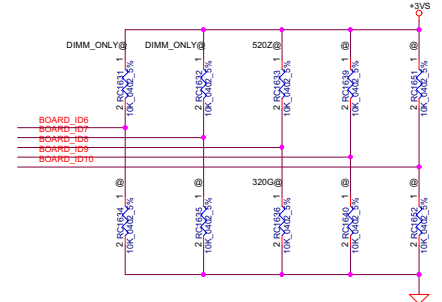
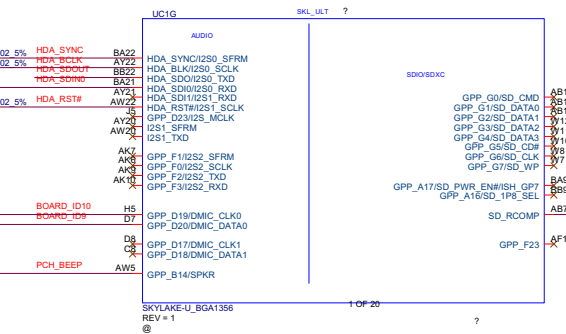
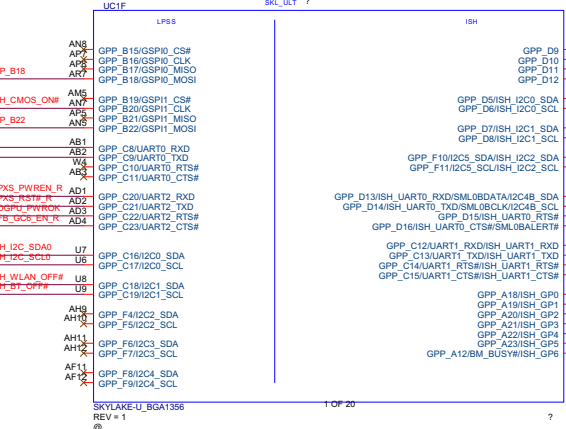
@UMA SKU



HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override).
This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
CSPI0 MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode.	0	Rising edge of PCH_PWROK
CSPI1 MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK



Board ID	Description	Stuff R
Board_ID [6,7]	00 Samsung 8Gb 2400 Mt/s	RC1634 RC1635
	01 Hynix 8Gb 2400 Mt/s	RC1634 RC1632
	10 Micron 8Gb 2400 Mt/s	RC1631 RC1635
	11 SO-DIMM Only	RC1631 RC1632
Board_ID8	0 320G	RC1636
	1 5202	RC1633
Board_ID9	0 Reserved	RC1640
	1 Reserved	RC1639
Board_ID10	0 Reserved	RC1652
	1 Reserved	RC1651

@DIS For NV and AMD GPU SKU



DGPU

LAN

WLAN

SATA HDD

SATA ODD

Optane Memory



UC1H

SKL_ULT ?

PCIE/USB3/SATA

SSIC / USB3

USB2

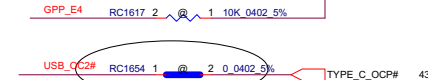
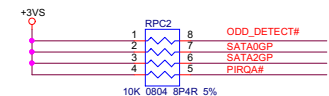
SKYLAKE-U_BGA1356

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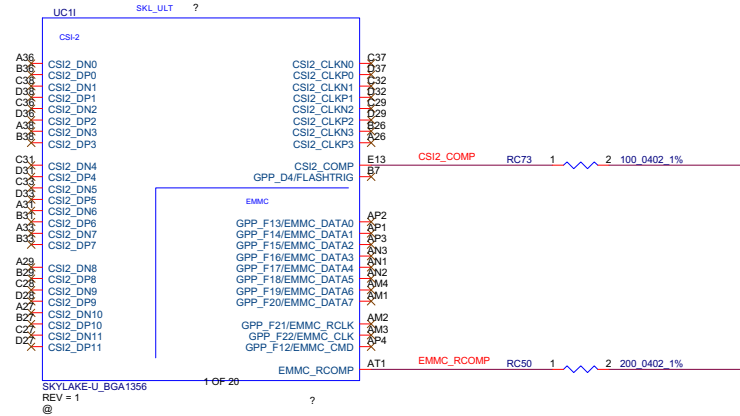
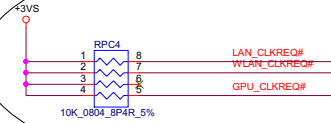


8/24 Reserve TYPE_C_OCP# to CPU USB_OC2# we

2016/05/03: Implement as Power Button function for Windows RedStone support

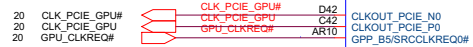
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check the Pull up resistor



@DIS For NV and AMD GPU SKU

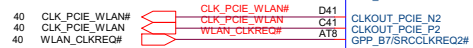
PCIE CLK0 DGPU



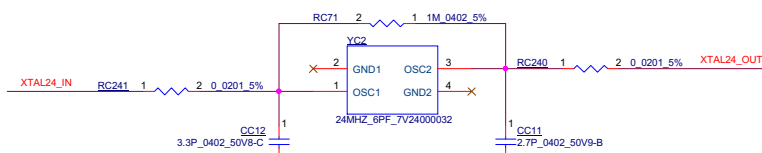
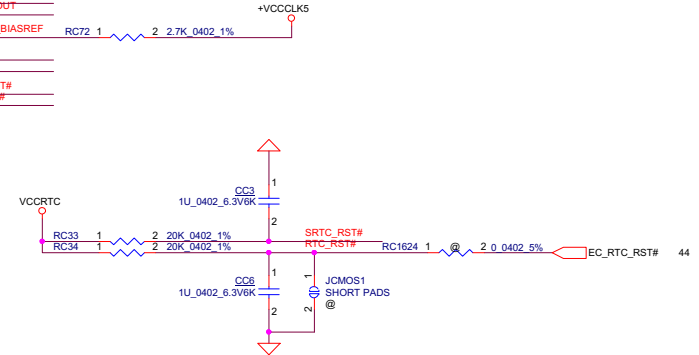
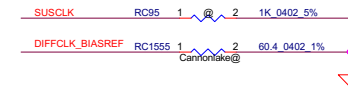
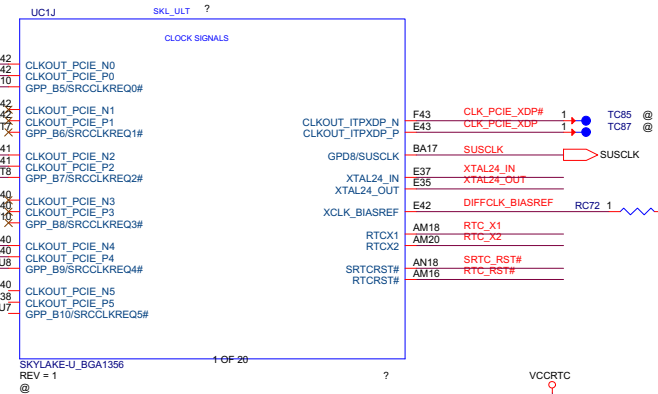
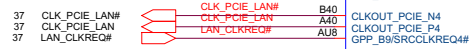
Optane memory



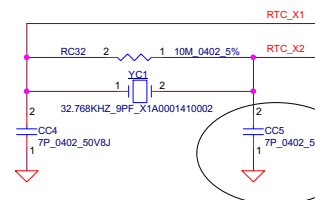
PCIE CLK5 WLAN



PCIE CLK4 LAN

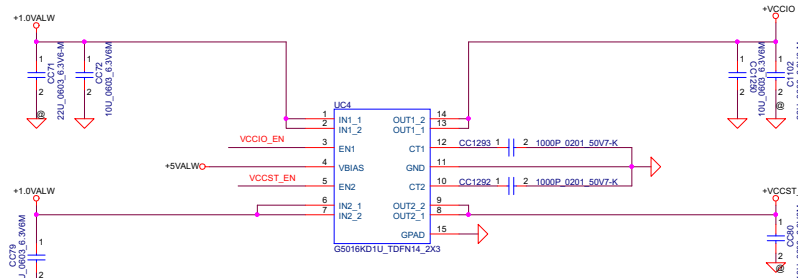
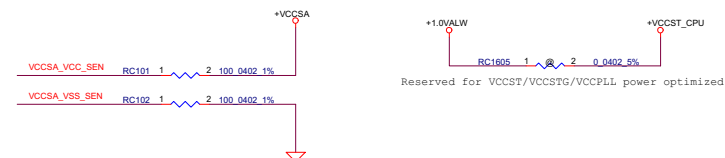
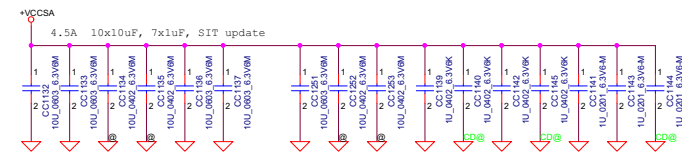


need to use 38.4MHz (30ohm) for Cannonlake-u

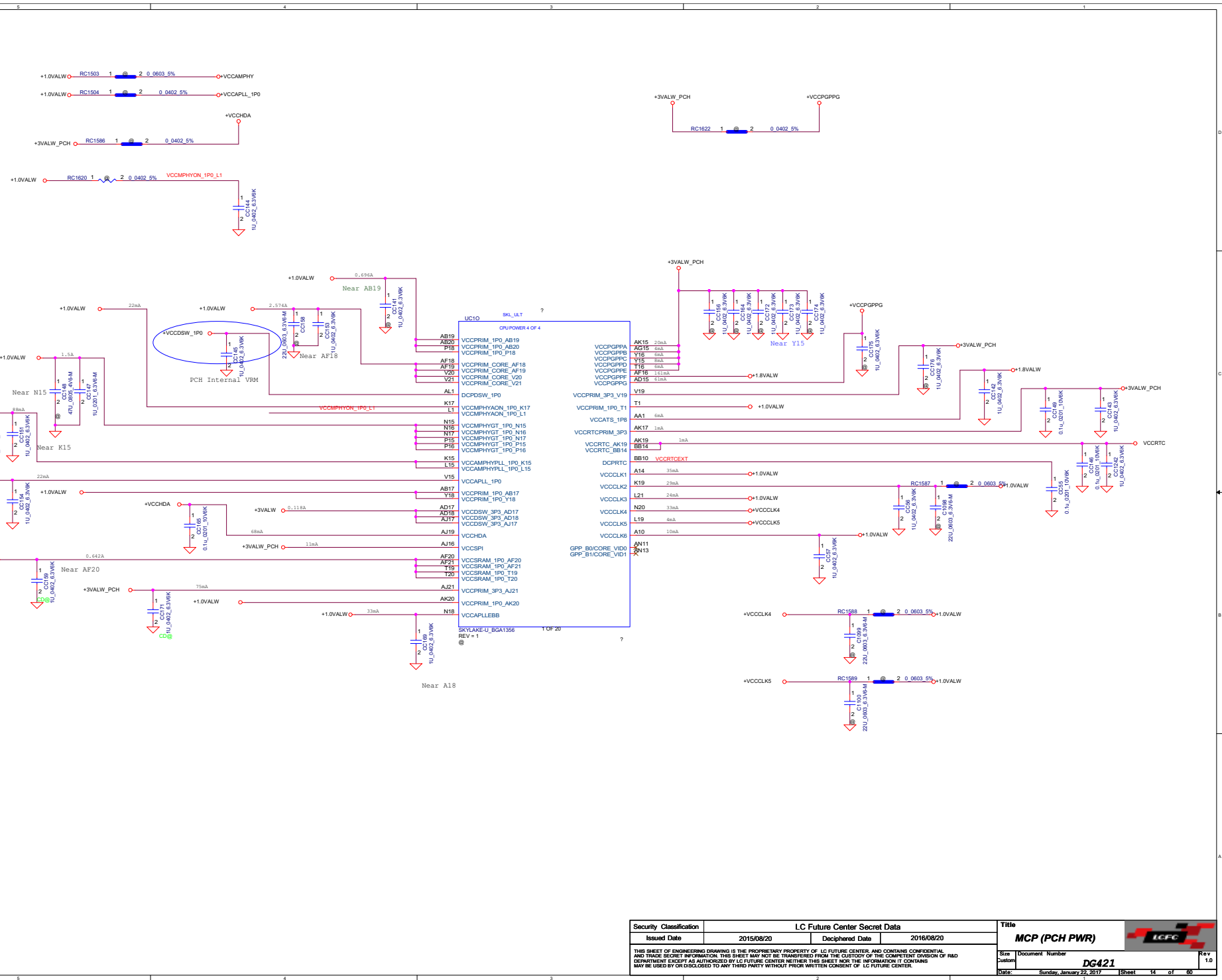



when single end external clock generator used, this pin should be grounded

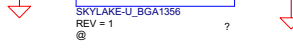
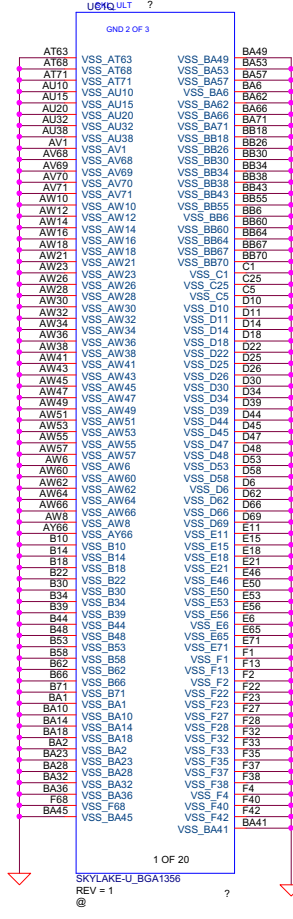
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Follow DG470 change to Dual Switch 8/24 wei

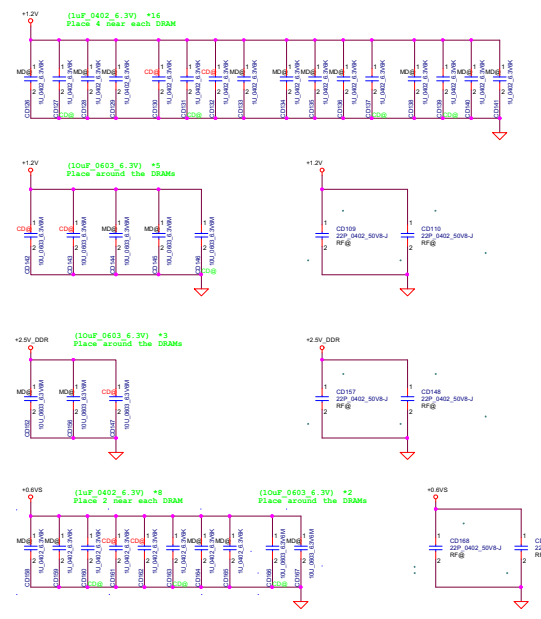
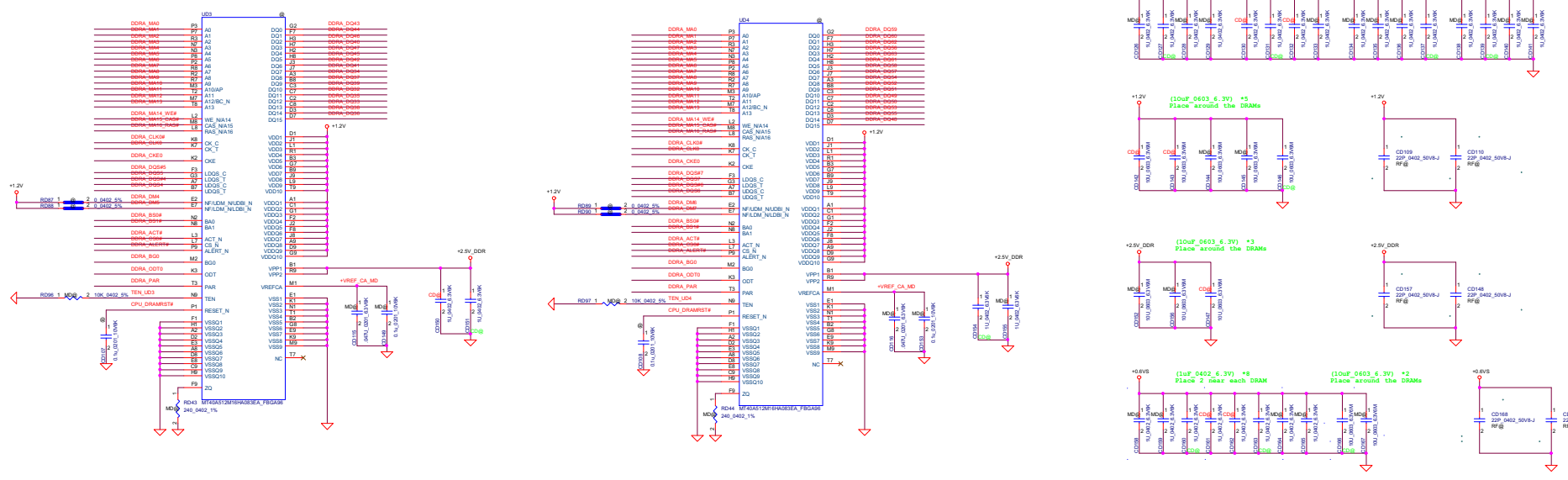
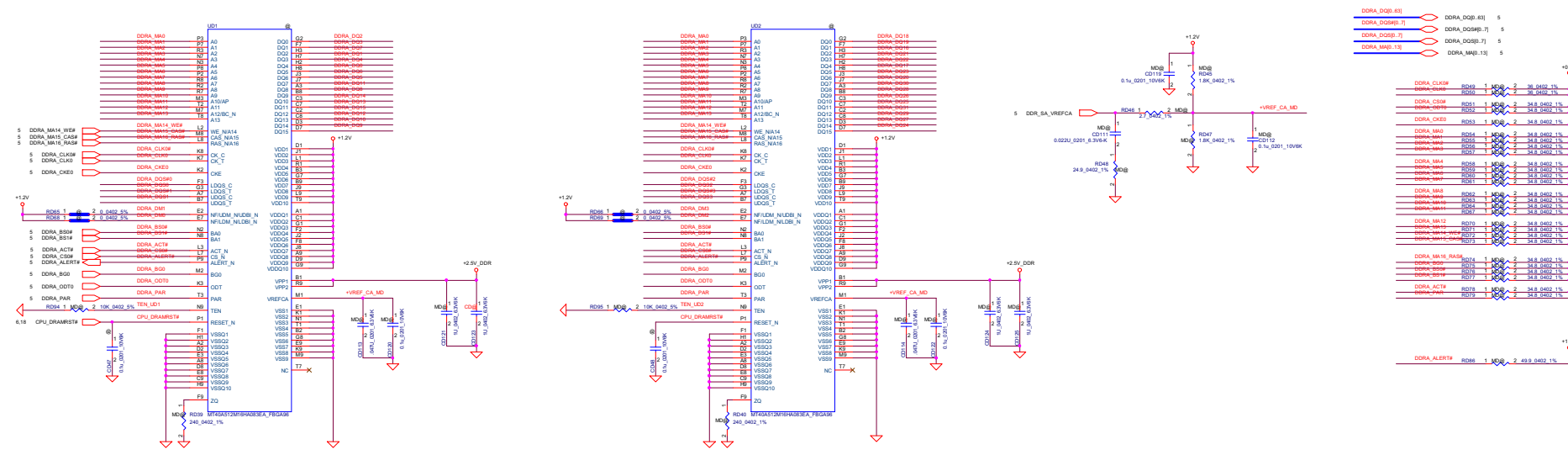
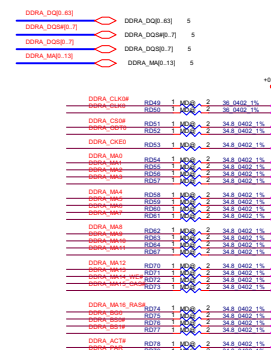


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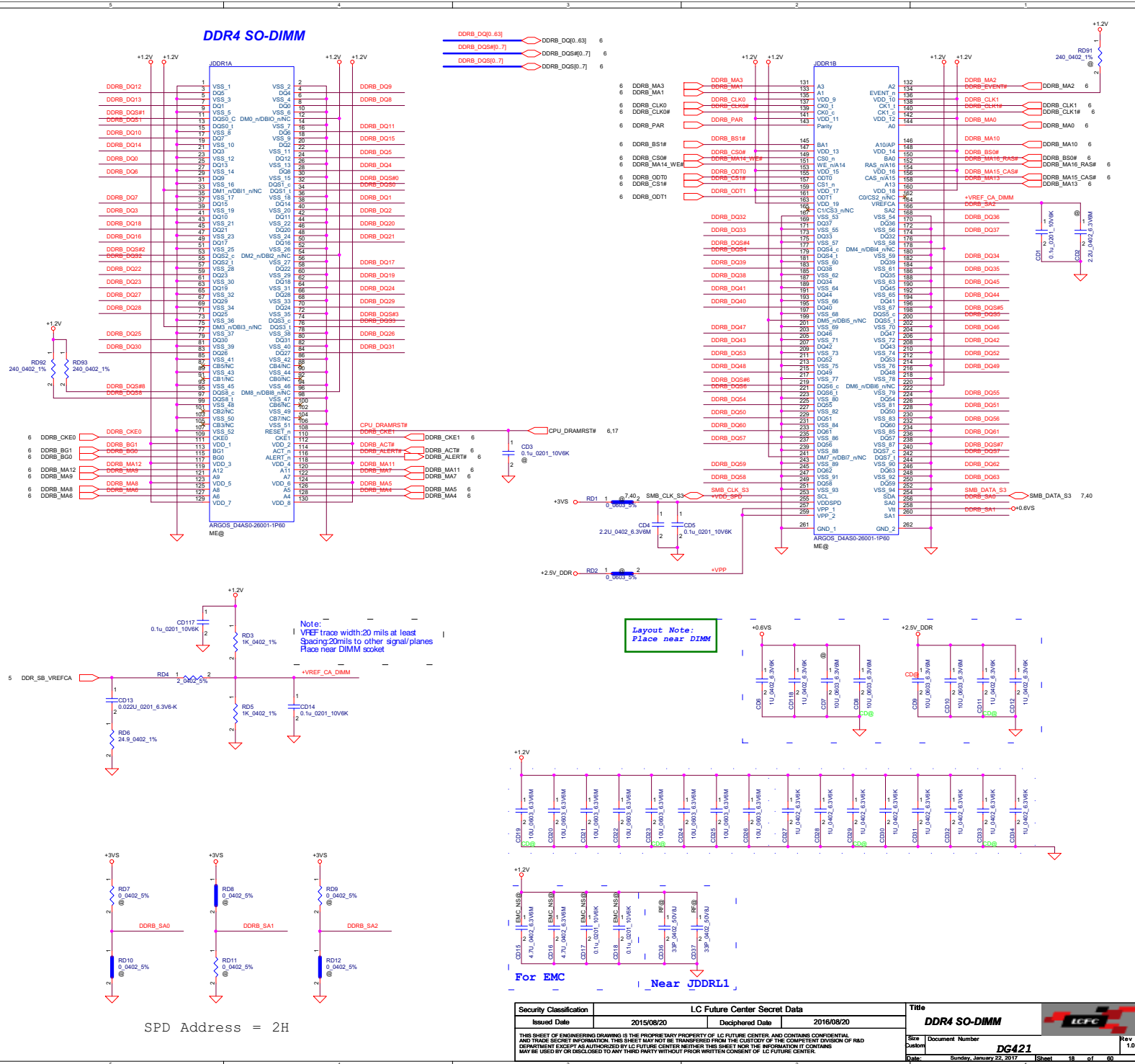


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			DDR4 Memory Down
			Rev. 1.0
			DC421



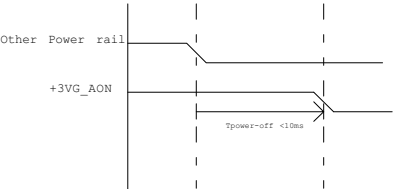
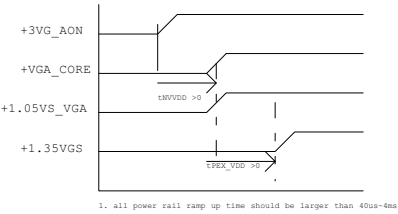
SPD Address = 2H

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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence

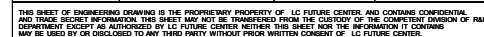


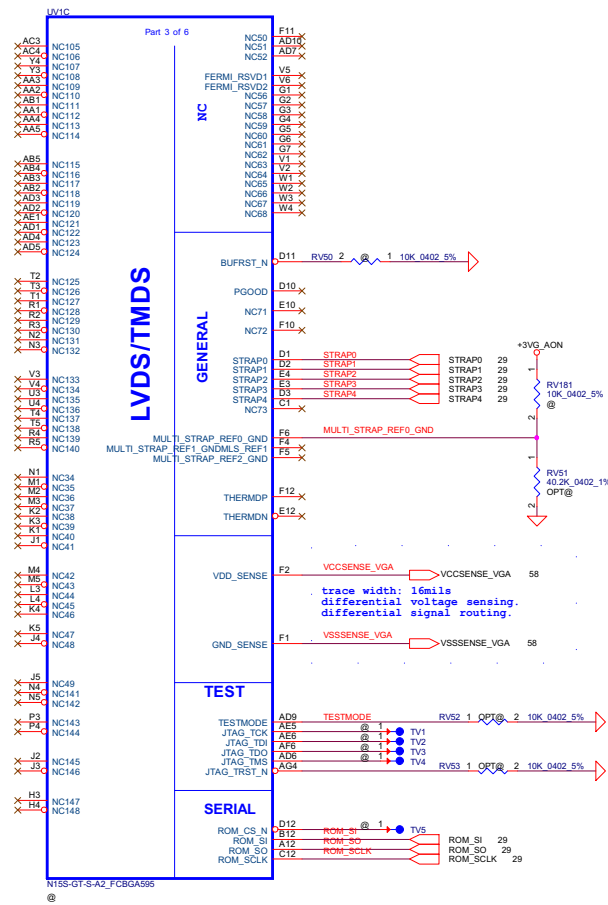
Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVDD (V)	(A)	(W)	FBVDD (1.35V) (A)	(W)	FBVDDQ (GPU+Mem) (1.35V) (A)	(W)	(1.05V) (6) (mA)	(W)	Other (3.3V) (mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

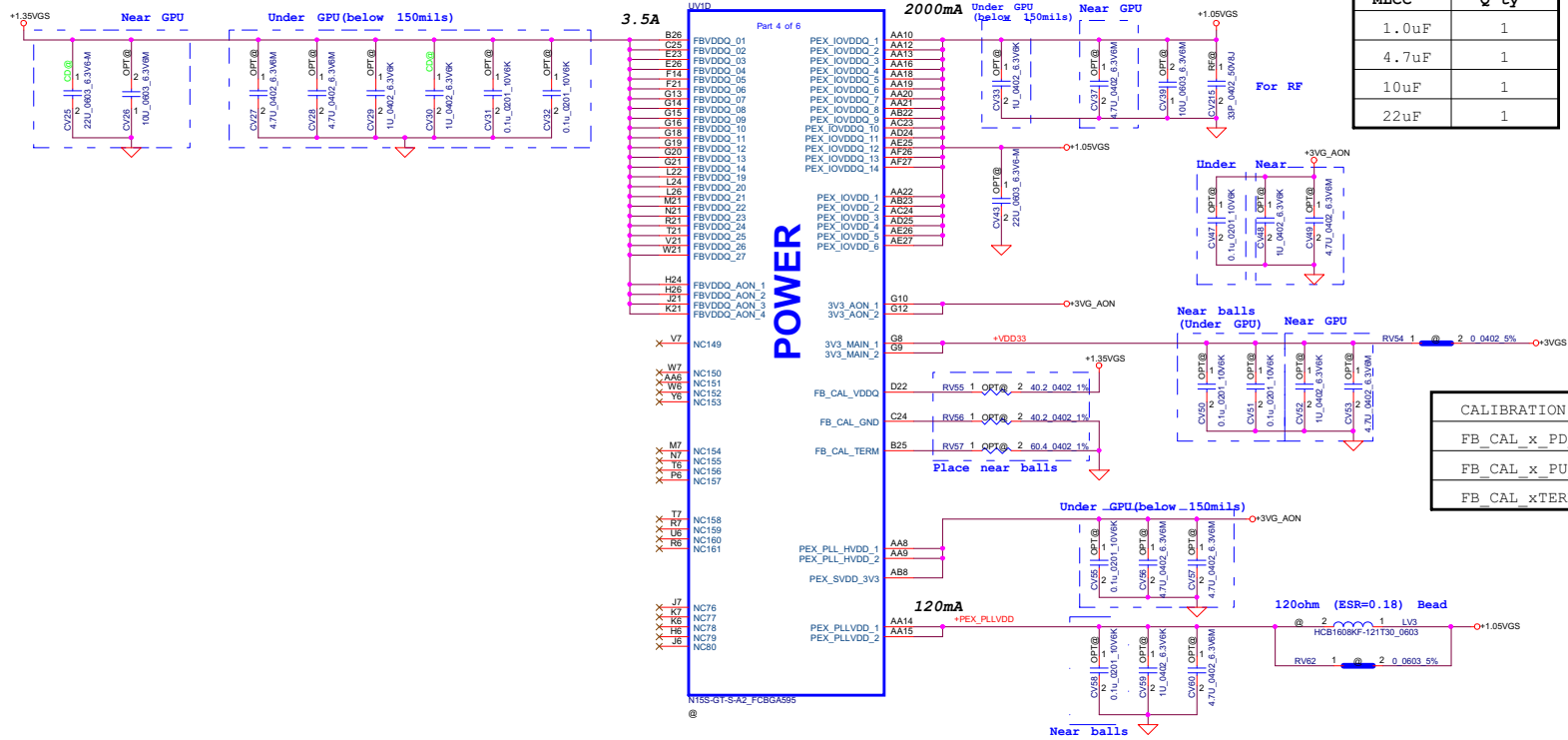
N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

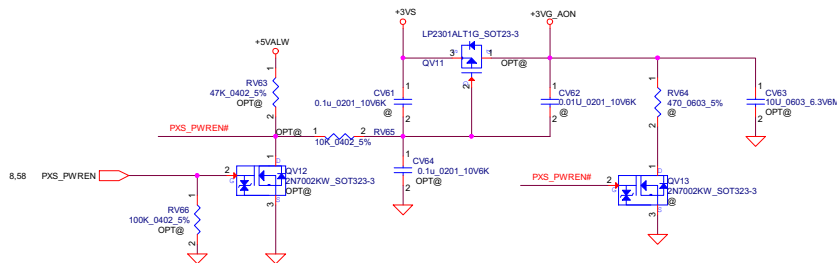




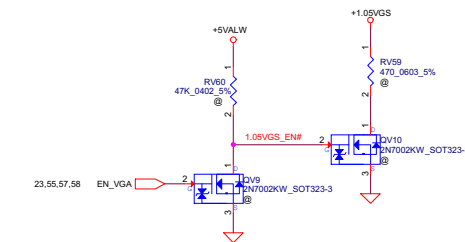
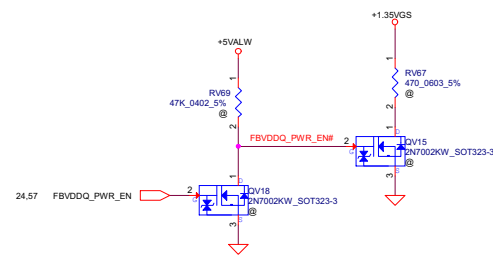
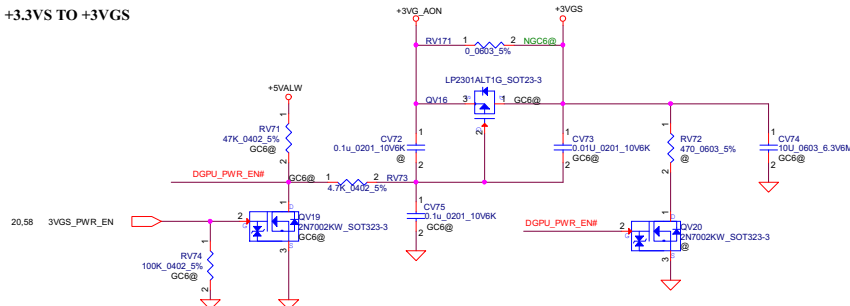
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	N16X_LVDS/ HDMI/ THERM ICFC	
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Size	Document Number		DG421		Rev 1.0
Date:	Sunday, January 22, 2017		Sheet	21	of 60

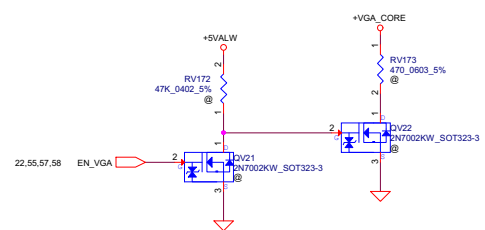
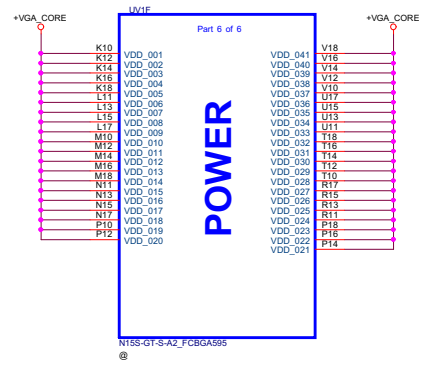
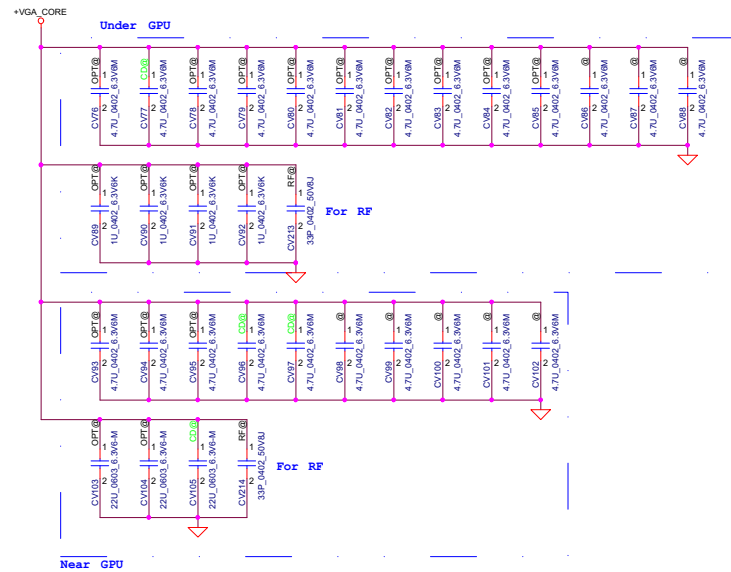
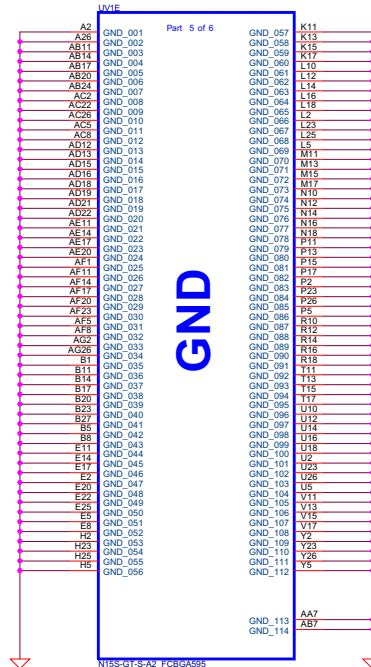


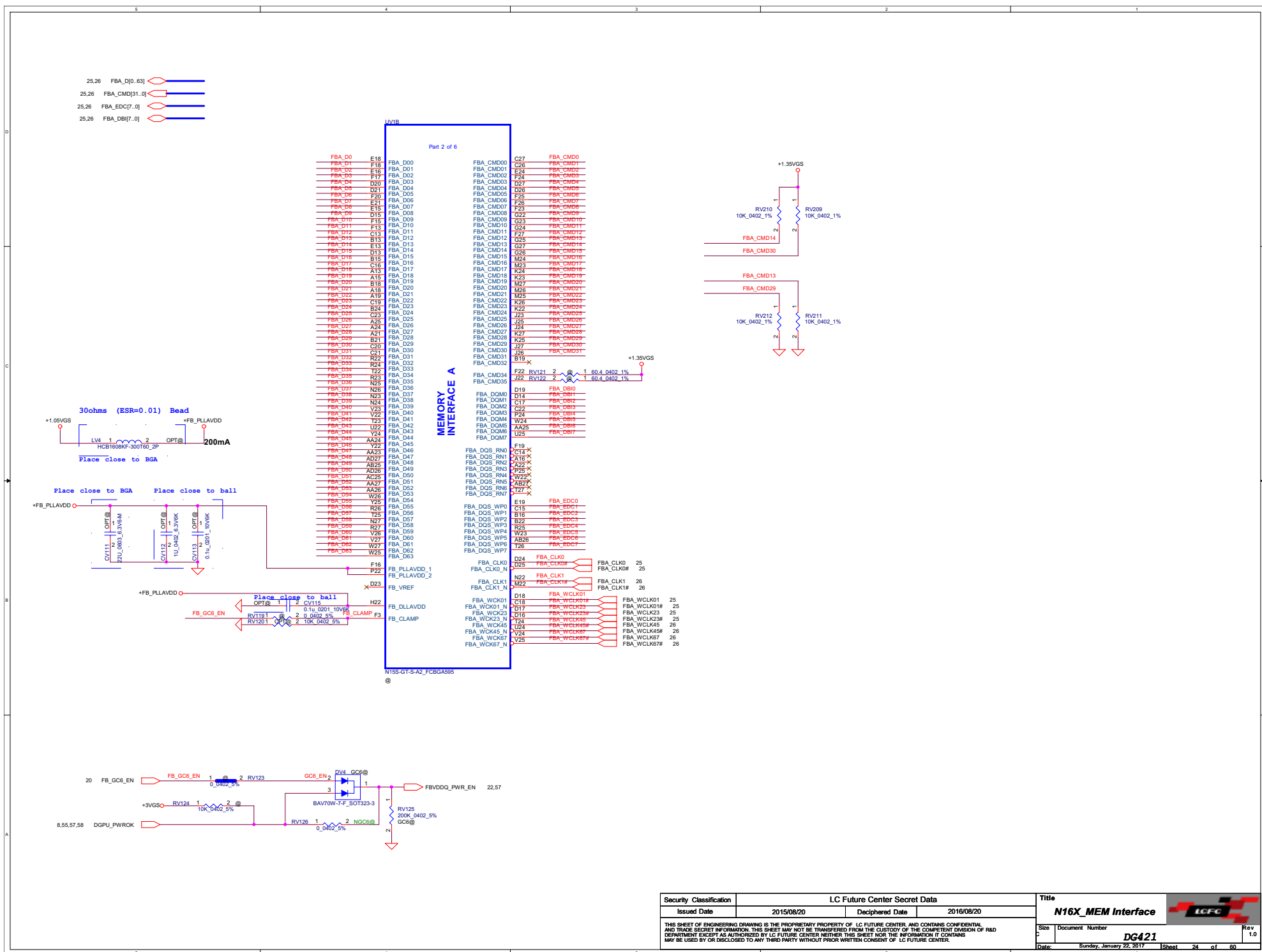
+3.3VS TO +3VG_AON





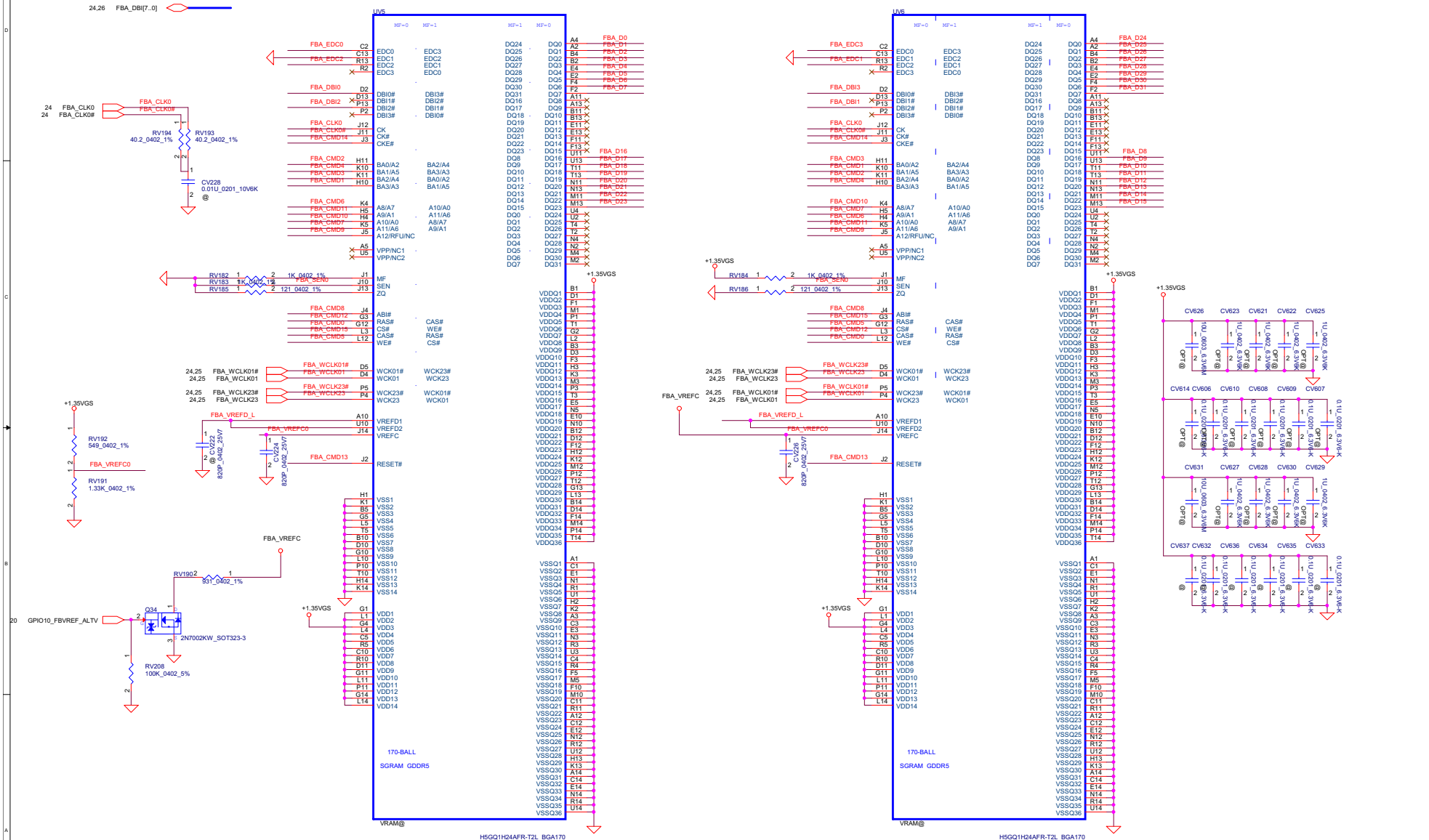
+3.3VS TO +3VGS






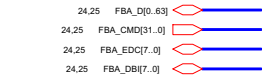


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Issued Date		Deciphered Date		N16X_MEM Interface			
2015/08/20		2016/08/20					
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Date				Sunday, January 22, 2017		Sheet 24 of 60	

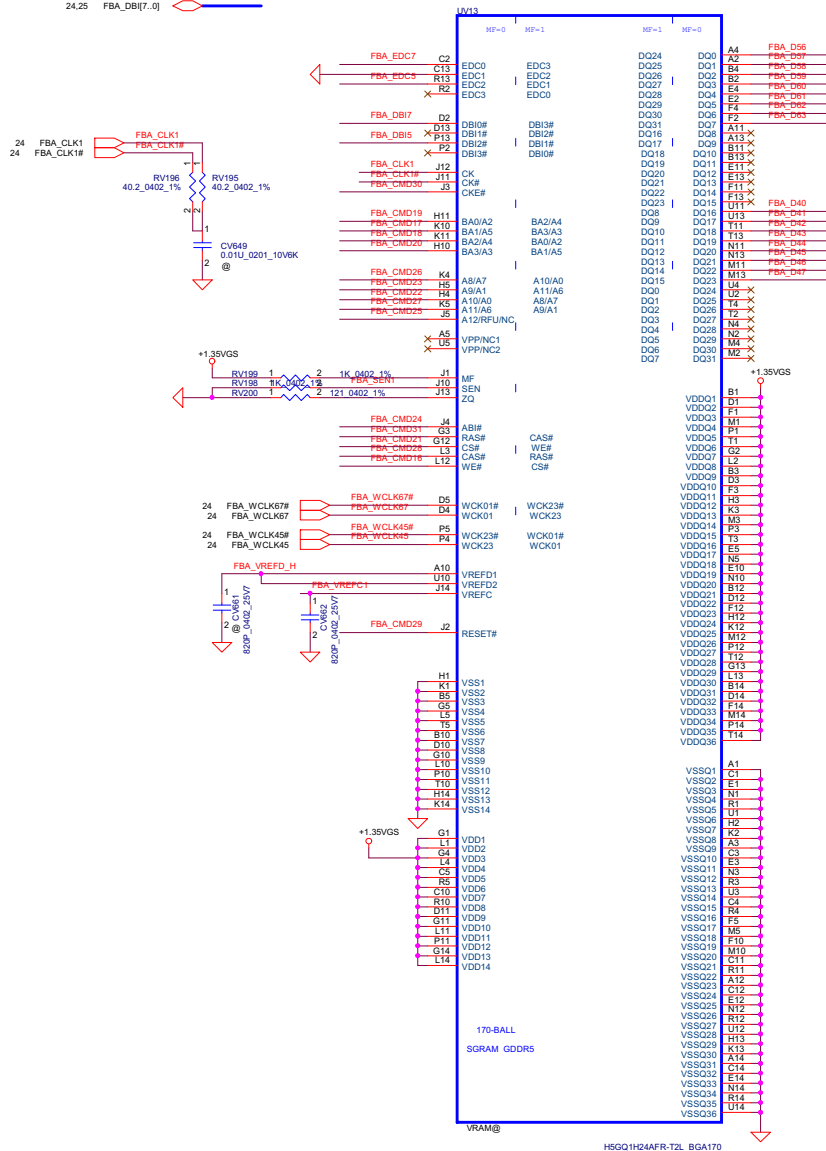
MF=1 Mirror

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Issued Date			2015/08/20			Deciphered Date			2016/08/20		
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Size						Document Number					
						DG421					
Date						Sunday, January 22, 2017					
Sheet						25 of 60					

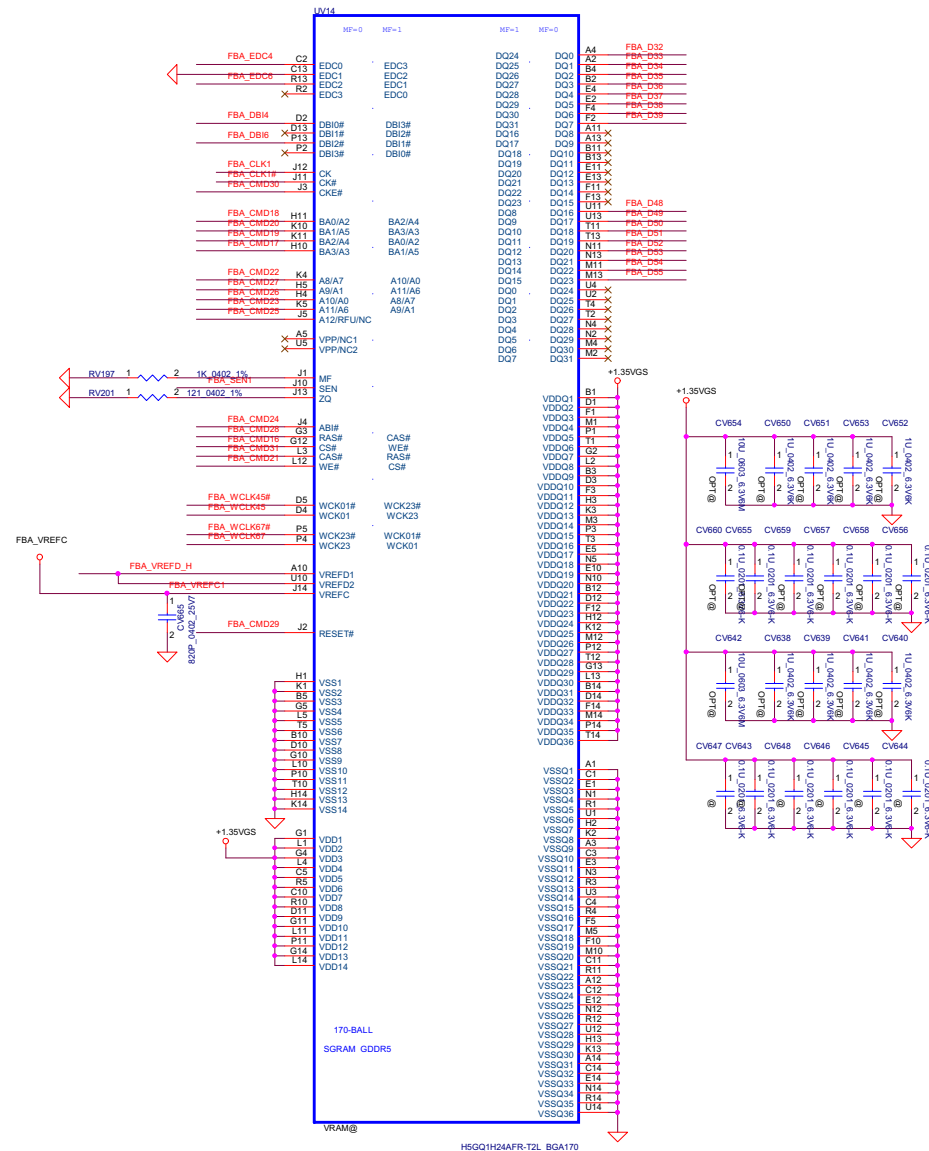
upper 32 bits




MF=1 Mirror




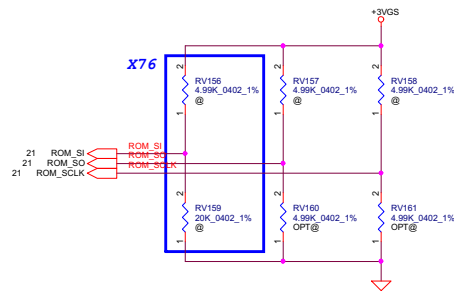
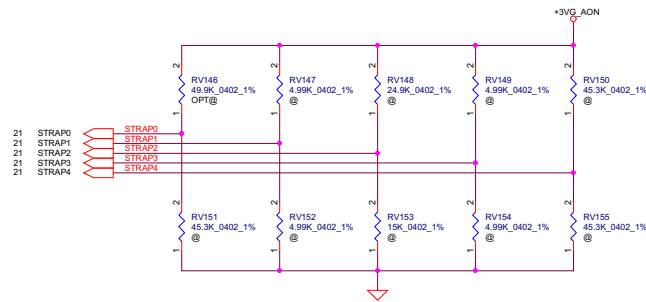
MF=0 No Mirror



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Issued Date	2015/08/20	Deciphered Date	2016/08/20	N16X_GDDR5_Rank0 [64:3] ICFO	
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Issued Date		2015/08/20		Deciphered Date		2016/08/20		N16X_DDR3_Rank1 [31:0] 	
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								Date: Sunday, January 22, 2017 Sheet 27 of 60	

Security Classification				LC Future Center Secret Data				Title	
Issued Date		2015/08/20		Deciphered Date		2016/08/20		N16X_DDR3_Rank1_16432 	
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								Date: Sunday, January 22, 2017 Sheet 28 of 60	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

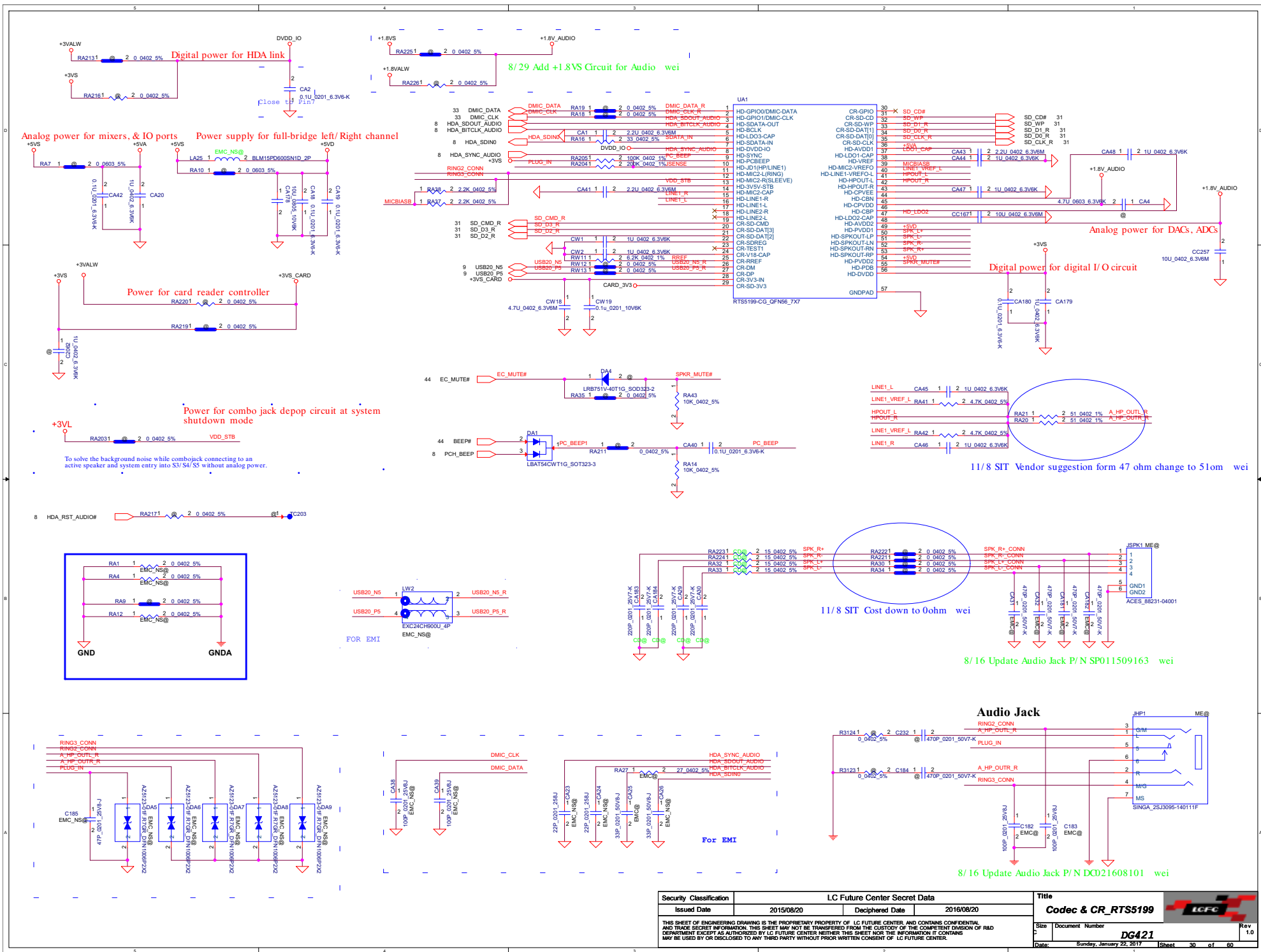
DEVID_SEL	
0	(Default)
1	

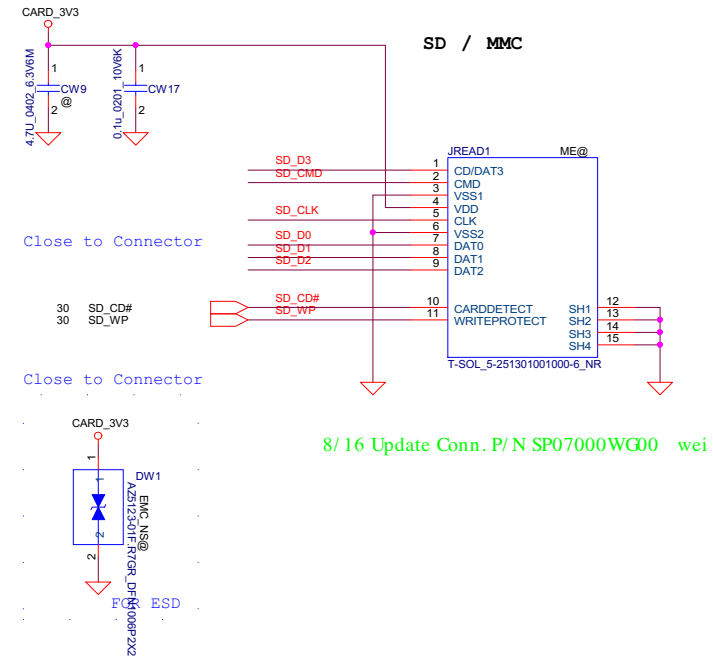
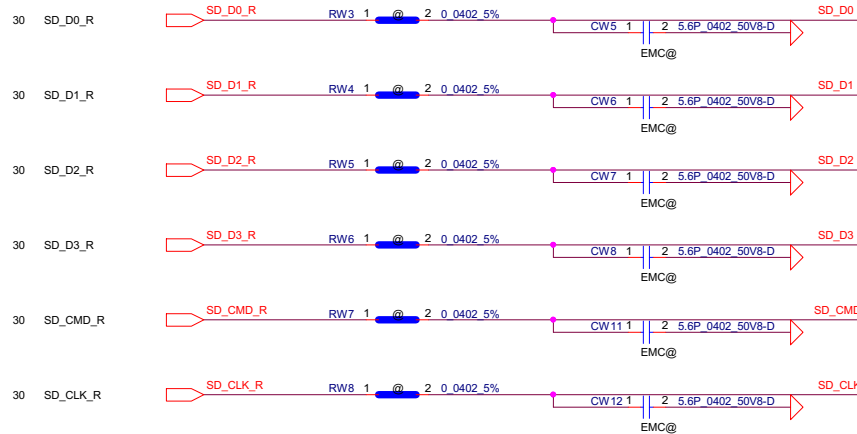
PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

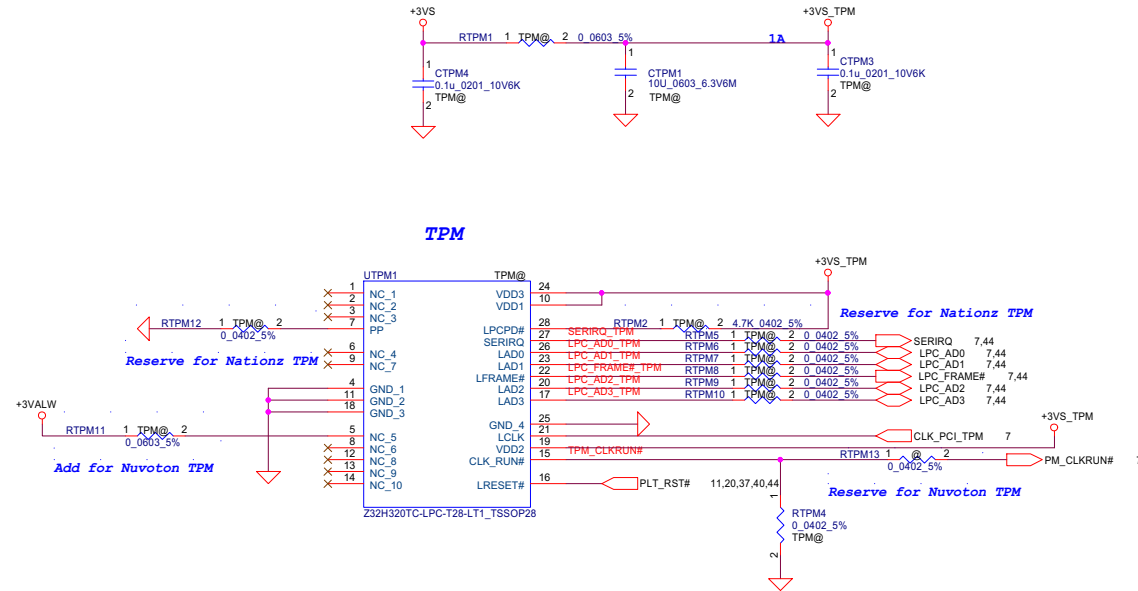
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	2G VRAM	Samsung 2500MHz K4G41325FE-HC28	0x7	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 45.3K							
		H5GC4H24AJR-T2C	0x6							
		256M x 16	PD 34.8K							
		EDW4032BABG-60-F	0x4							
		256M x 16	PD 24.9K							
	4G VRAM	Samsung 2500MHz K4G80325FB-HC03	0x0							
		512M x 16	PD 4.99K							
		H5GC8H24MJR-T2C	0x5							
		512M x 16	PD 30.1K							
		MT51J256M32HF-60-A	0x1							
		512M x 16	PD 10K							





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				Rev	1.0



	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

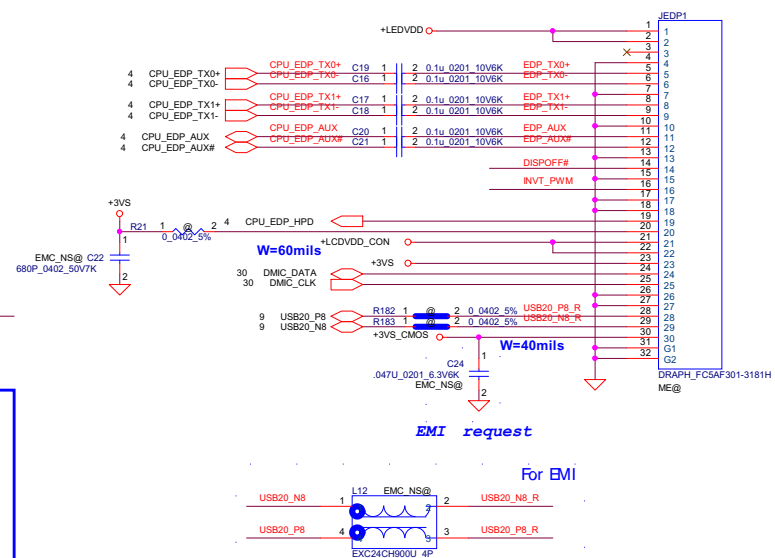
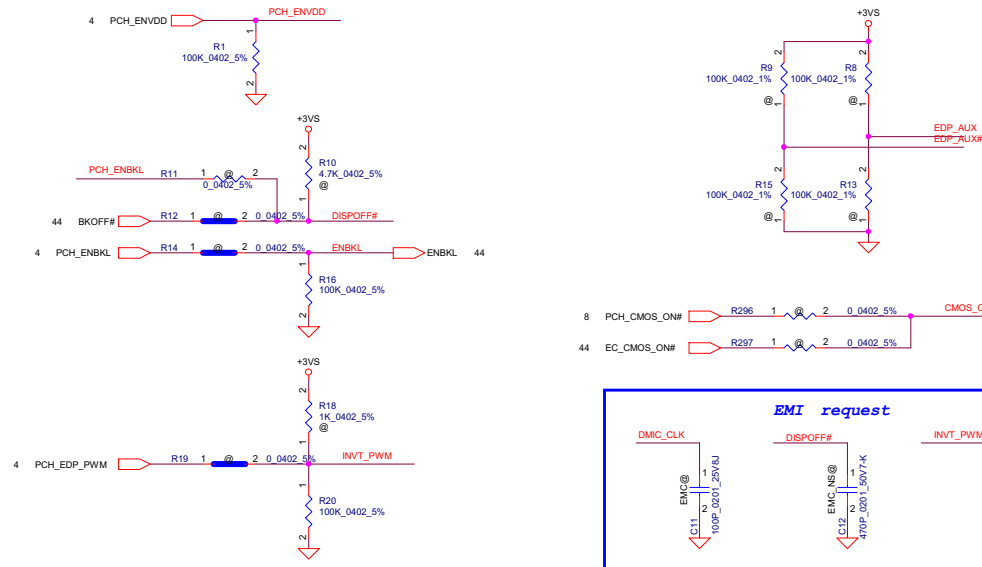
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Issued Date	2015/08/20	Deciphered Date	2016/08/20
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Rev	1.0		

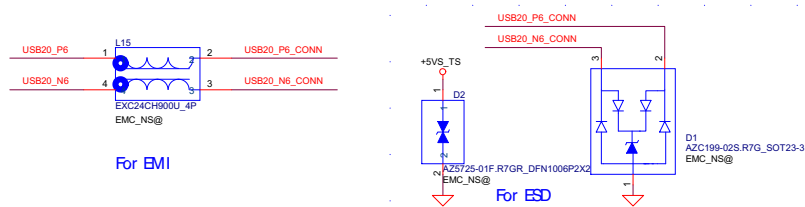
[illegible]


The diagram shows a 4-layer PCB layout for a CMOS camera interface. Key components and annotations include:

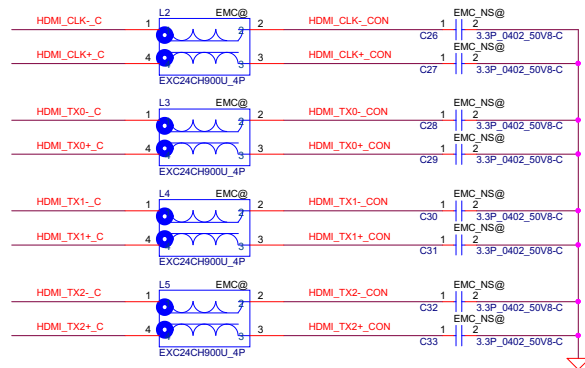
- CMOS Camera** (top left): A blue label indicating the camera module's location.
- Need short** (top center): A blue label indicating a required short circuit.
- W=40 mils** (top left): A dimension indicating the width of a trace.
- W=40mils** (top right): A dimension indicating the width of a trace.
- Components:**
 - J1**: A connector labeled "J1" with a note "JUMP_43X39".
 - LP2301ALT1G_SOT23-3**: A buffer IC.
 - Q7**: A MOSFET.
 - R3**: A resistor labeled "0.1u020_10V6K".
 - C3**: A capacitor labeled "0.1u_0201_10V6K".
 - C4**: A capacitor labeled "100J_0603_6.3V5M".
 - C5**: A capacitor labeled "0.1u_0201_10V6K".
 - C9**: A capacitor labeled "0.01u_0201_25V6-K EMC_NS@".
 - C10**: A capacitor labeled "0.1u_0201_10V6K".
 - R5**: A resistor labeled "100K_0402_5%".
- Power and Ground:**
 - +3VS**: Power supply input.
 - +3VS_CMOS_R**: Power supply input.
 - +3VS_CMOS**: Power supply input.
 - CMOS_ON#**: A control signal input.
- Annotations:**
 - For EMI Close to R5**: A note indicating the placement of capacitor C9 for EMI reduction.
 - 0.01u_0201_25V6-K EMC_NS@**: A note indicating the placement of capacitor C9 for EMI reduction.



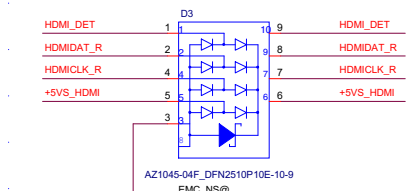
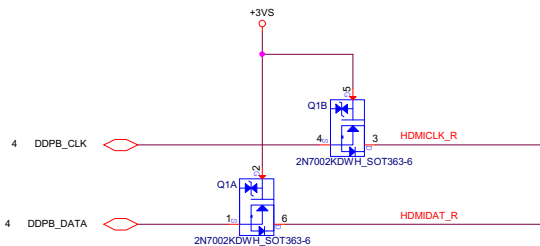
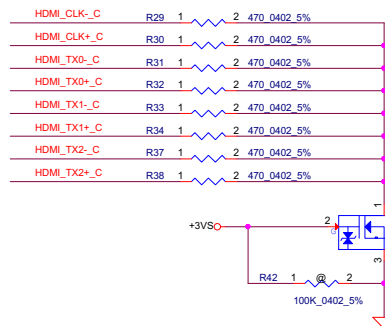
Touch Screen



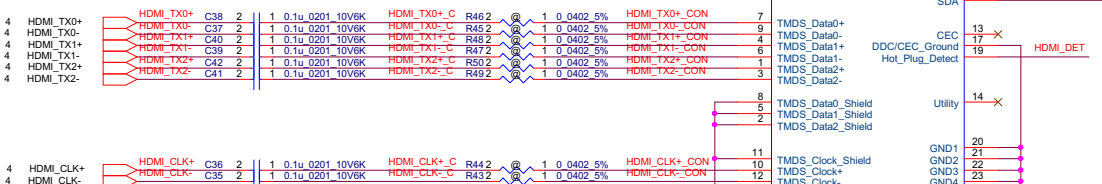
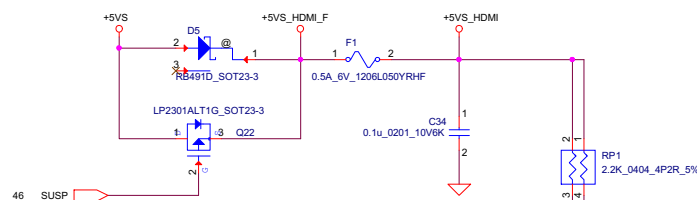
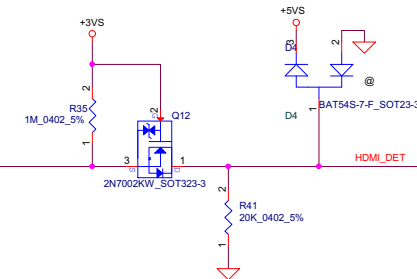
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For EMC

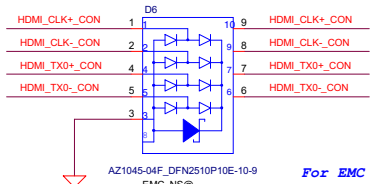


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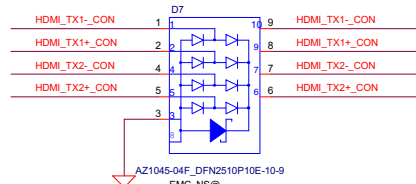



8/16 Update HDMIConn.P/N DCD21608081 wei

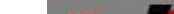
Close to JHDMI1



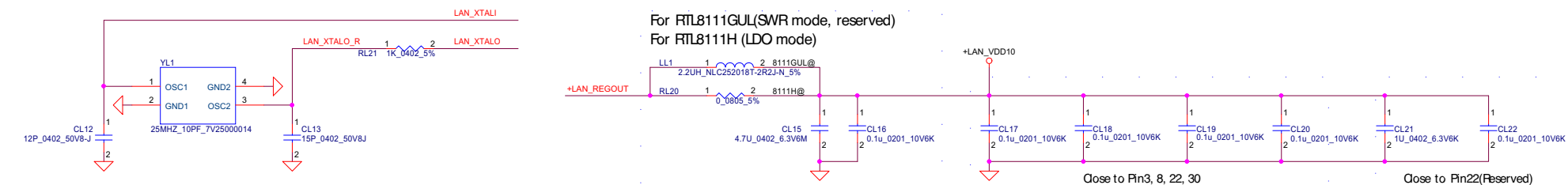
For EMC



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5		4		3		2		1	
D									
C									
B									
A									
								</	

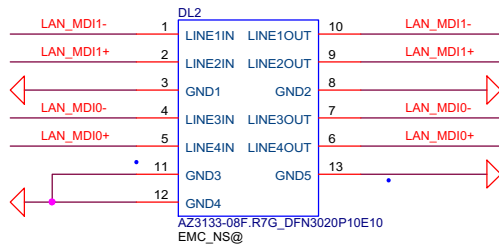
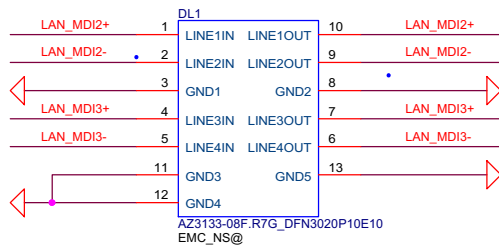


For RTL8111G(LSWR mode, reserved)
For RTL8111H (LDO mode)

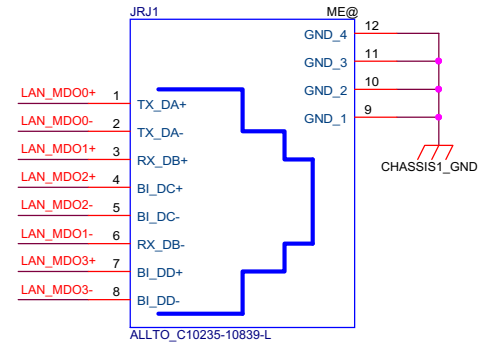
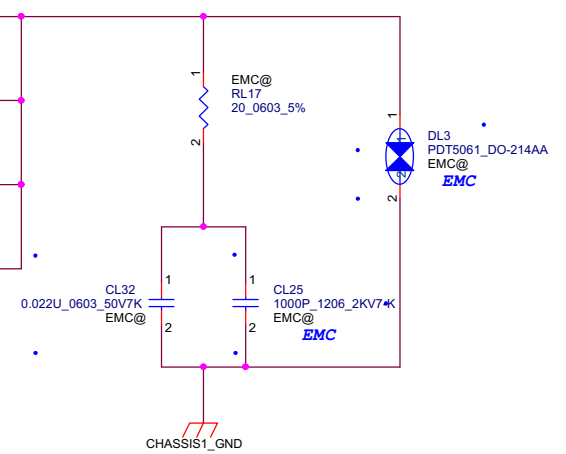
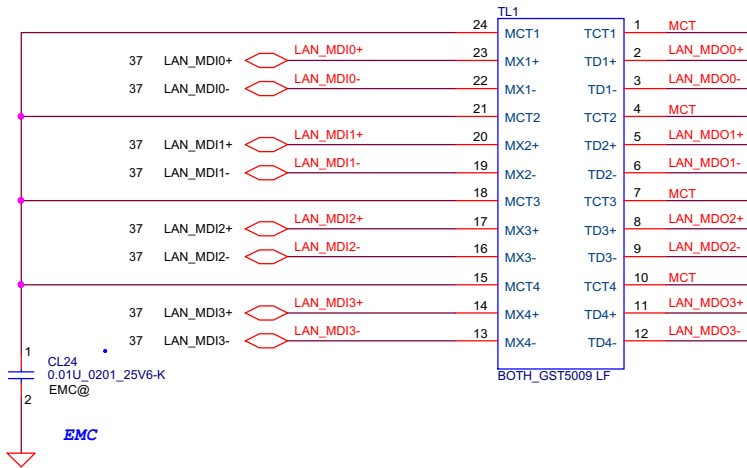
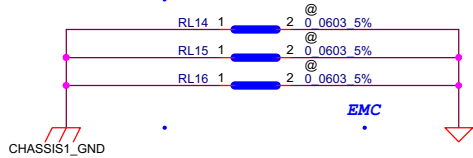
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN REGOUT: Width =60mil

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_RTL8111H_CG	
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				Date: Sunday, January 22, 2017 12:00 PM Sheet 37 of 60	Rev 1.

DL1/DL2 1'S PN:SC300003M00



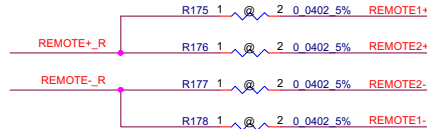
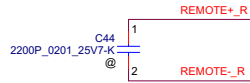
Place Close to TL1



8/16 Update R45 P/N DC021608091 wei

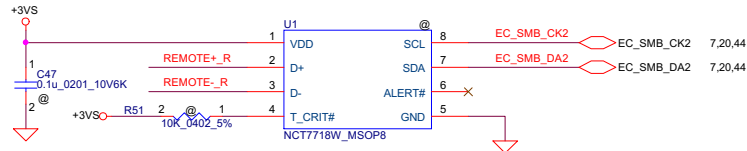
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_Transformer	
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Close to U1

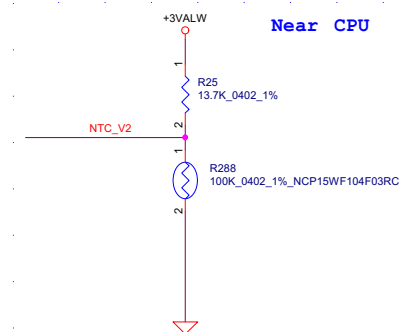
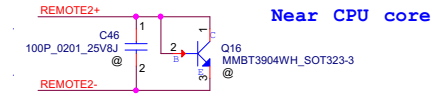
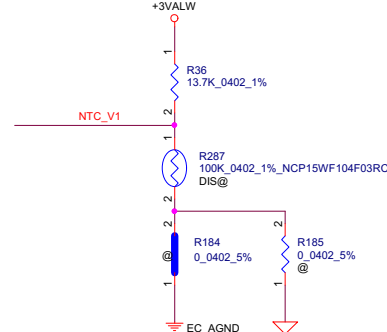
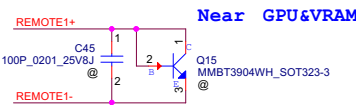


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

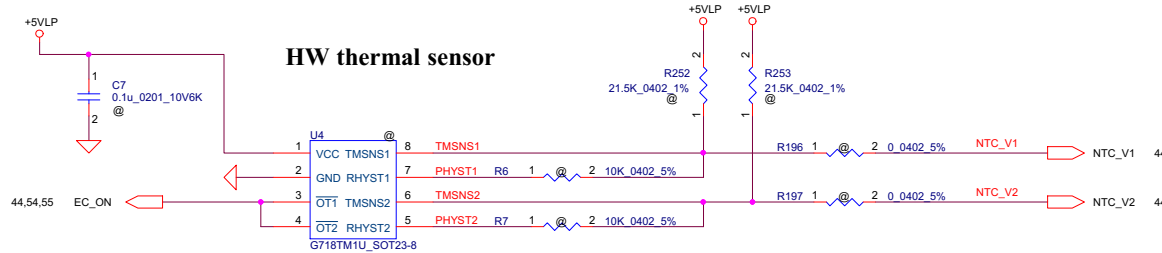


Address 1001_101xb

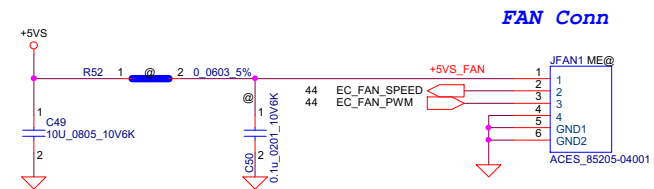


for layout optimized, change the EC_AGND to GND

HW thermal sensor



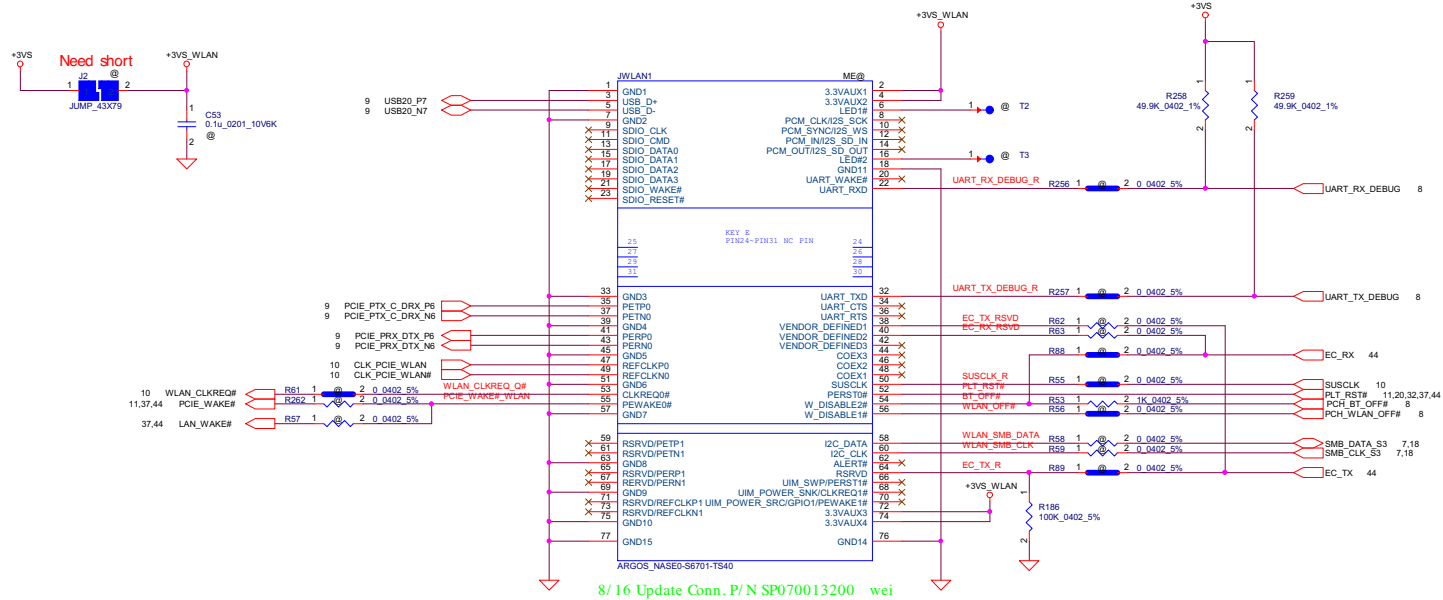
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



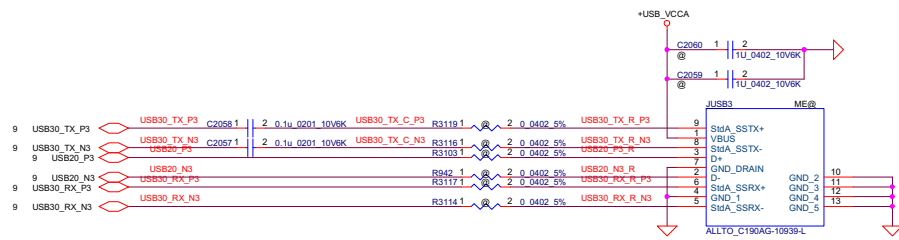
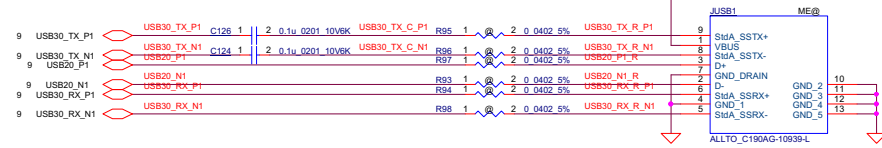
Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15
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Title		Thermal sensor/FAN Conn	
Size	Document Number	DG421	
Custom			
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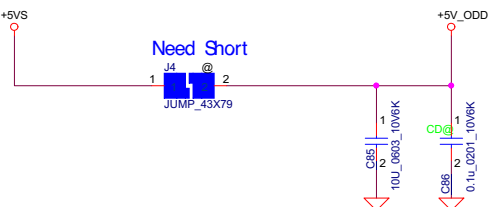
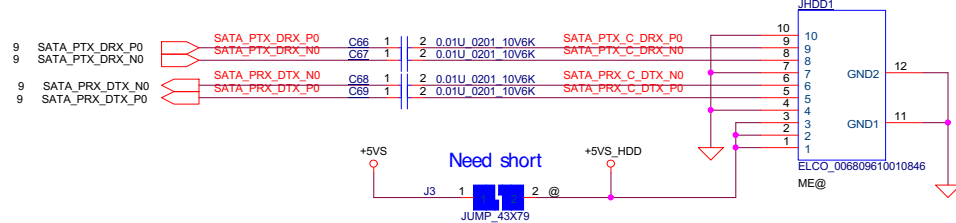
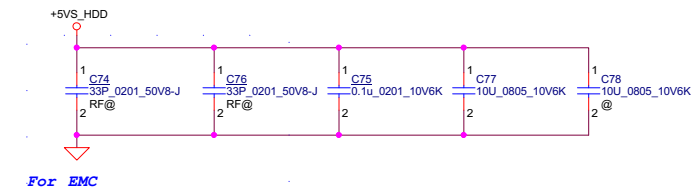
Mini-Express Card(WLAN/WiMAX)



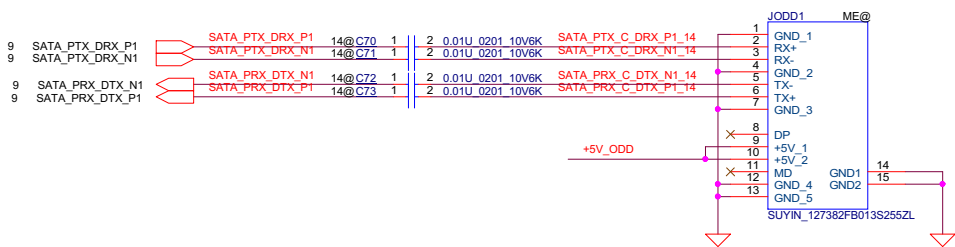
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	NGFF WLAN&SSD	
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					DG421
				Date	Sunday, January 22, 2017
				Sheet	40 of 60
				Rev	1.0



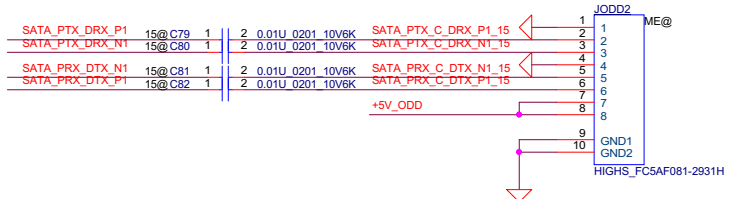
SATA HDD Conn.



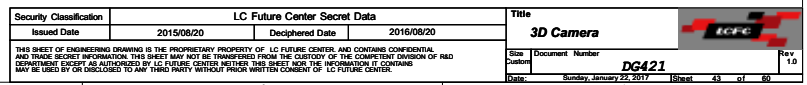
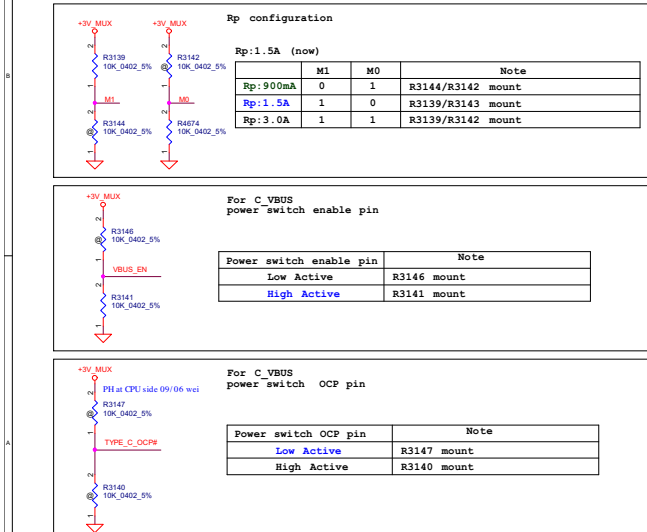
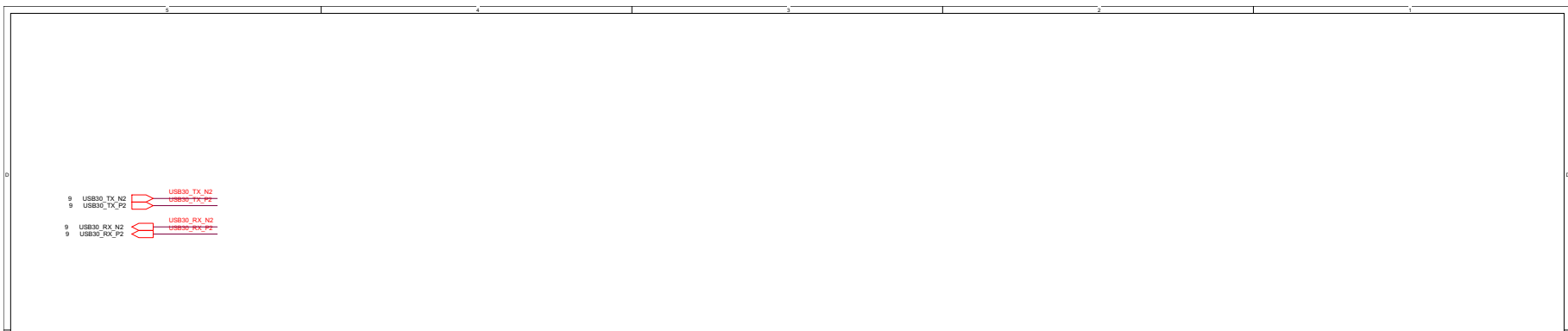
FOR 14" SATA ODD Conn.

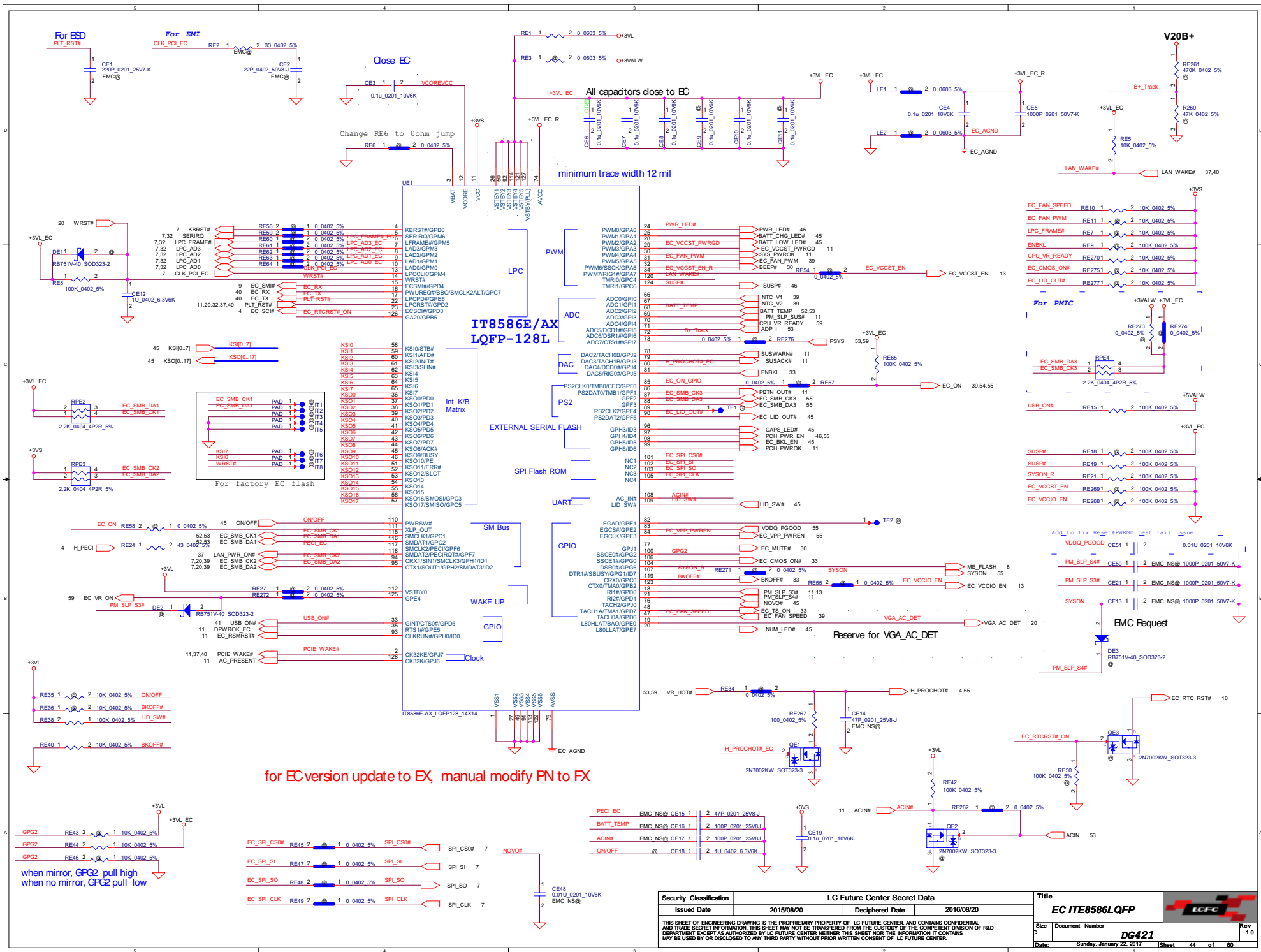


FOR 15" 17" SATA ODD FFC Conn

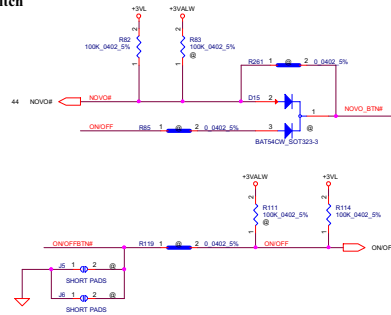


8/16 Update Conn. P/N SP01001YV00 wei

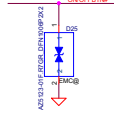




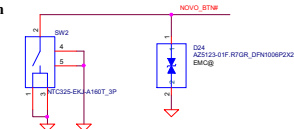
ON/OFF switch



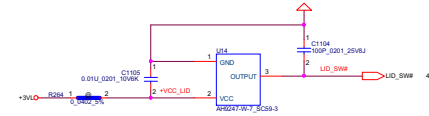
8/ 16 Del Power Button wei



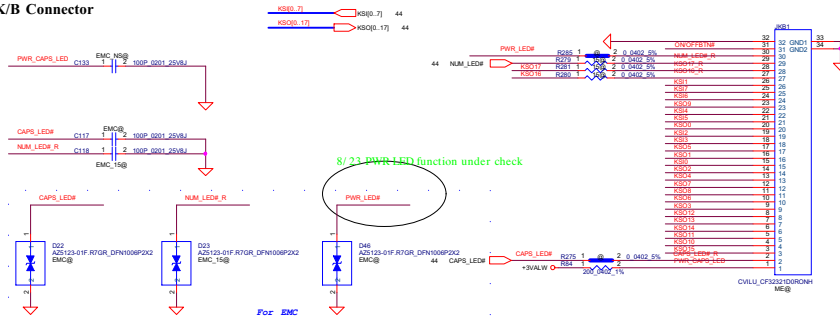
Novo button



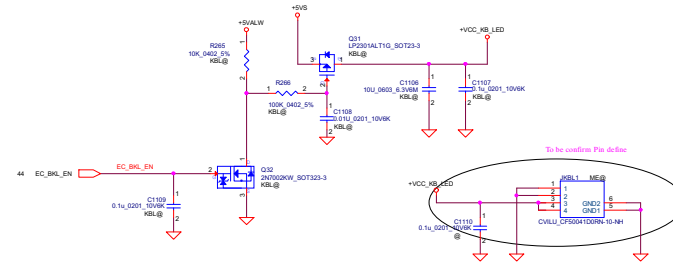
8/31 Update the P/N SN100008W00 wei

LID switch

K/B Connector

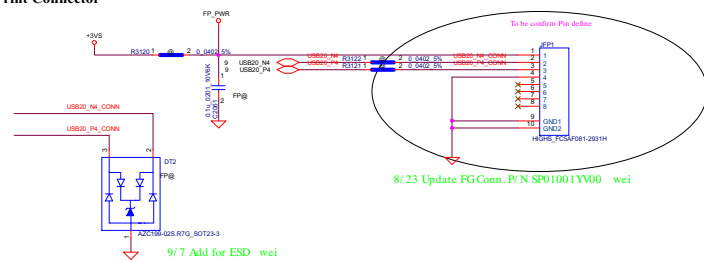


8/ 23 PWR LED function under check

KB Backlight Connector

8/31 Update KBL Conn. P/N SP011608241 wei

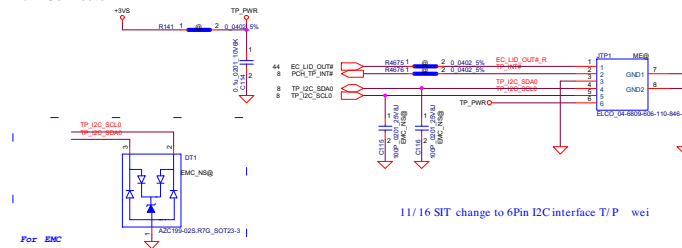
Finger Print Connector



8/23 Update FG Conn. P/ N SP01001YV00 wei

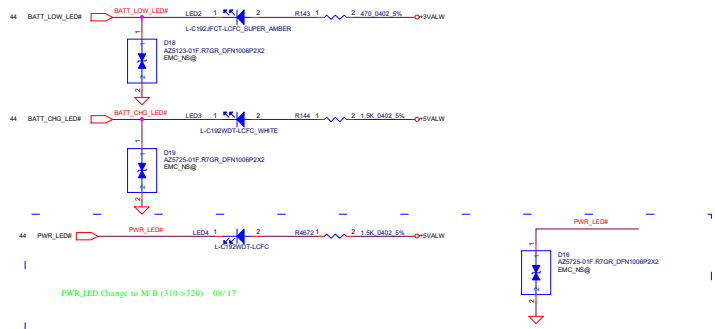
9/7 Add for ESD wei

TP/B Connector




11/16 SIT change to 6Pin I2C interface T/P wei

For EMC



PWR_LED Change to M/B (310->320) 08/17

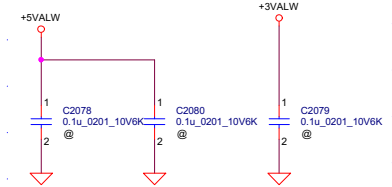
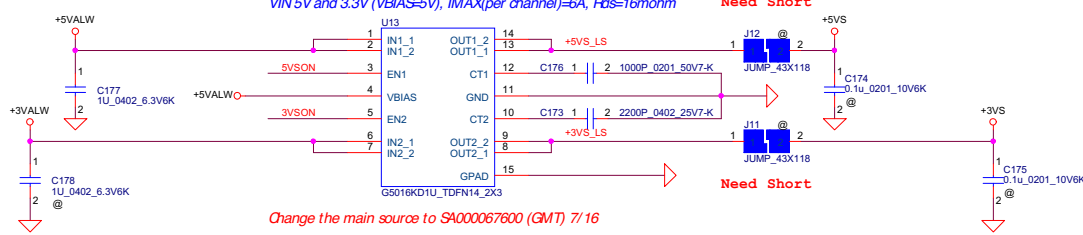
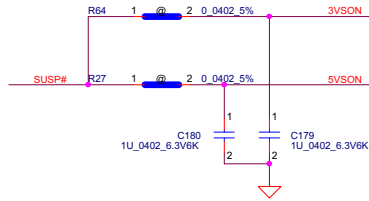
Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/08/20	Deciphered Date	2015/08/20
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Size	Document Number		DG421

Load Switch
+5VALW To +5VS
+3VALW To +3VS

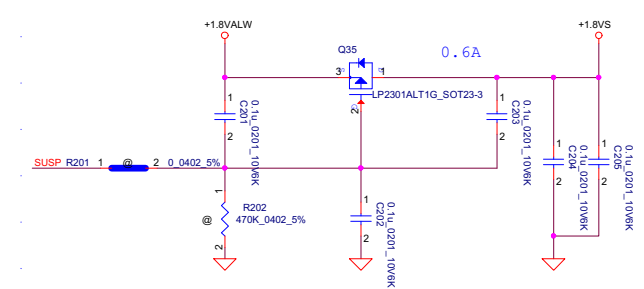
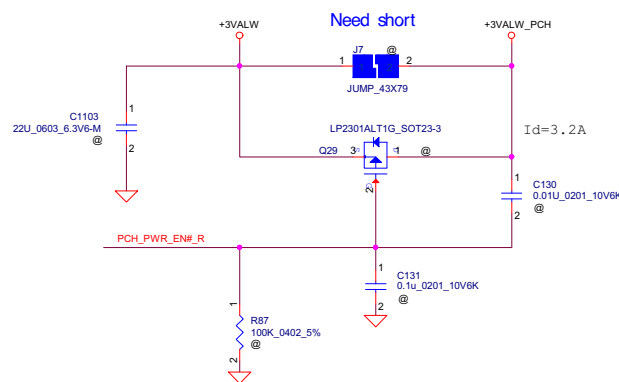
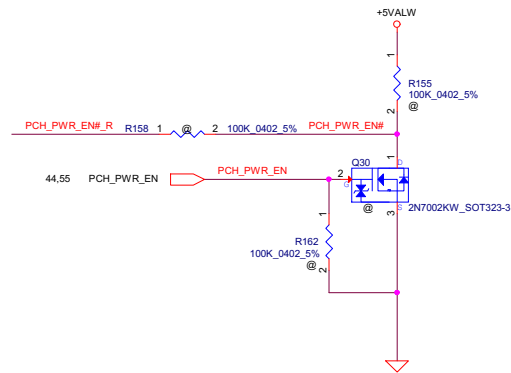
+3VS C173 --> 2.74ms
+5VS C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

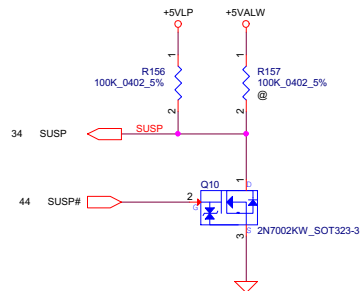
Need Short



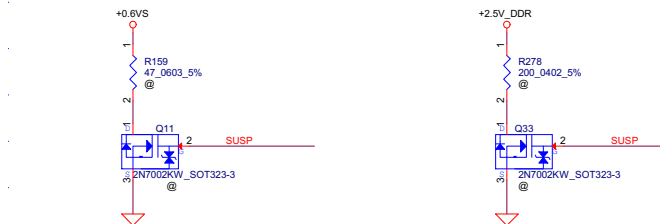
EMC




8/29 Add +1.8VS Circuit for Audio wei

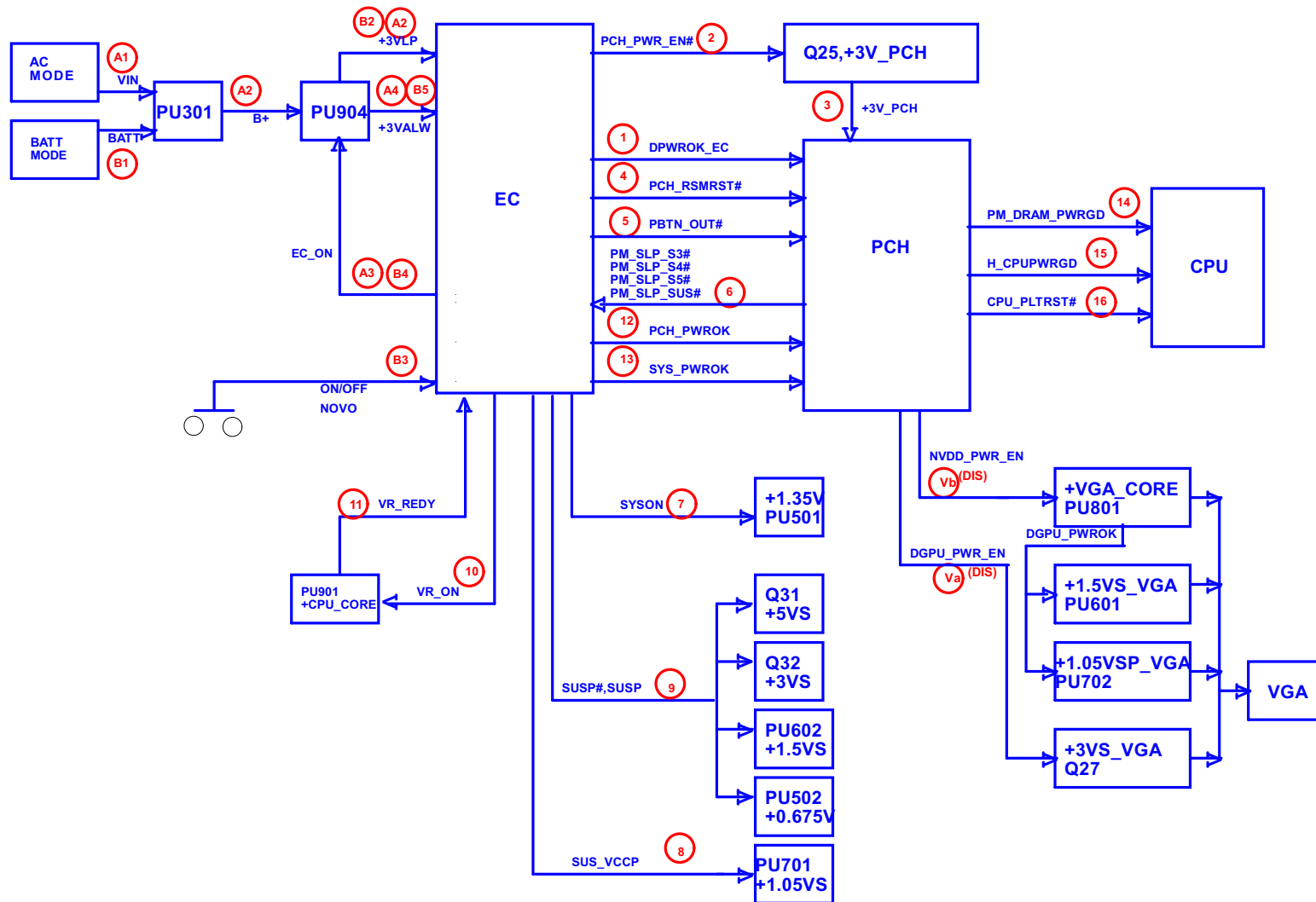


For DisCharge




08/29: Need double check enable signal and the resistance

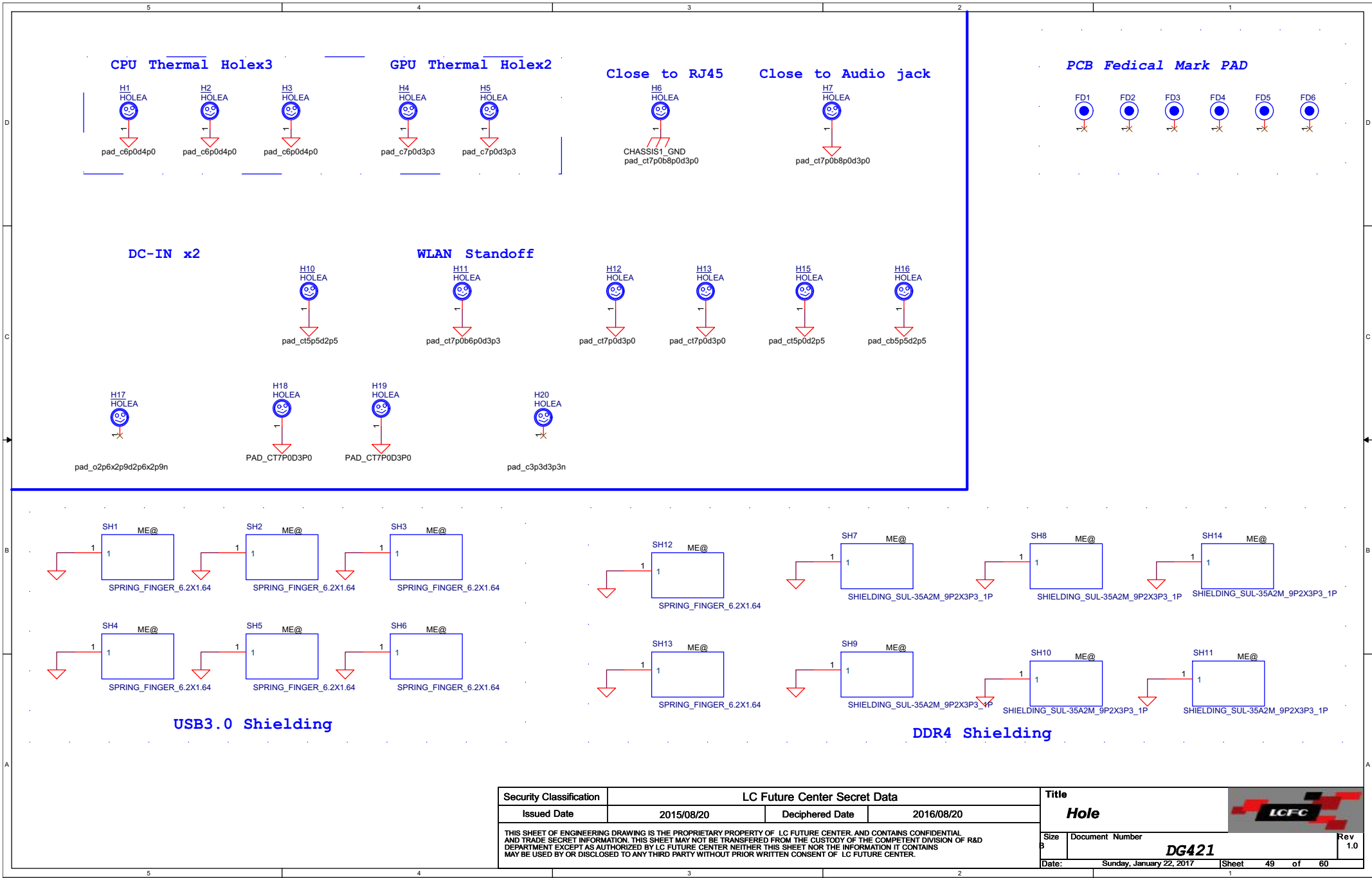
Security Classification	LC Future Center Secret Data			Title	DC V to VS INTERFACE 
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Size	
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				Custom	1.0
				Date:	Sunday, January 22, 2017
				Sheet	46 of 60

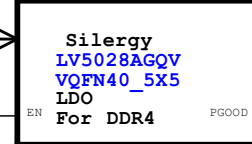
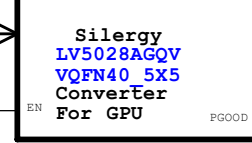
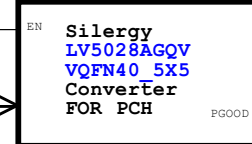
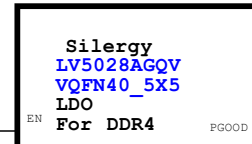
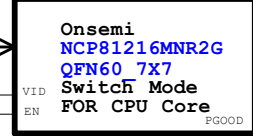
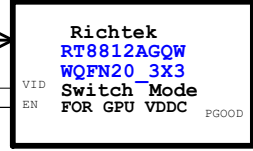
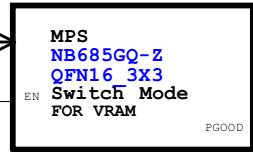
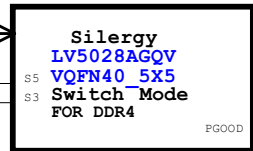
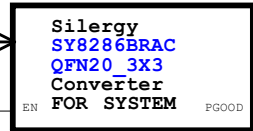
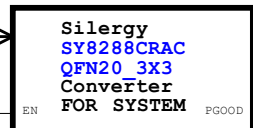
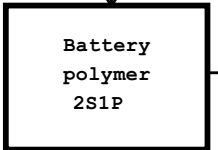
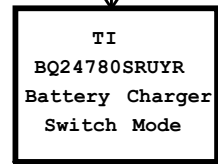
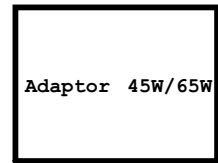


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Title		Power sequence block	
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Issued Date		2015/08/20		Deciphered Date			2016/08/20		Virtual symbol			
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								DG421		Date: Sunday, January 22, 2017		Sheet 48 of 60





EN_VGA

PCH_PWR_EN

PCH_PWR_EN

EC_VPP_PWREN

EC_ON

EC_ON

SYSON
CPU_DRAMPG_CNTL

FBVDDQ_PWR_EN

PXS_PWREN

EC_VR_ON

+1.05VGS/1.5A

PGOOD

+1.0VALW/6A

PGOOD

+1.8VALW/1A

PGOOD

+2.5V/1A

PGOOD

+5VLP/ 100mA

+5VALW/6A

+3VLP/ 100mA

+3VALW/ 5A

+1.2V/7A

+0.6VS/2A

+1.35V/8A

+VGA_CORE/31A

CPU Core/23A

VCCGT/25A

VCCSA/7A

CPU_VR_READY

PGOOD

PGOOD

PGOOD

PGOOD

PGOOD

PGOOD

NA

NA

NA

NA

NA

ALN_PWRGD

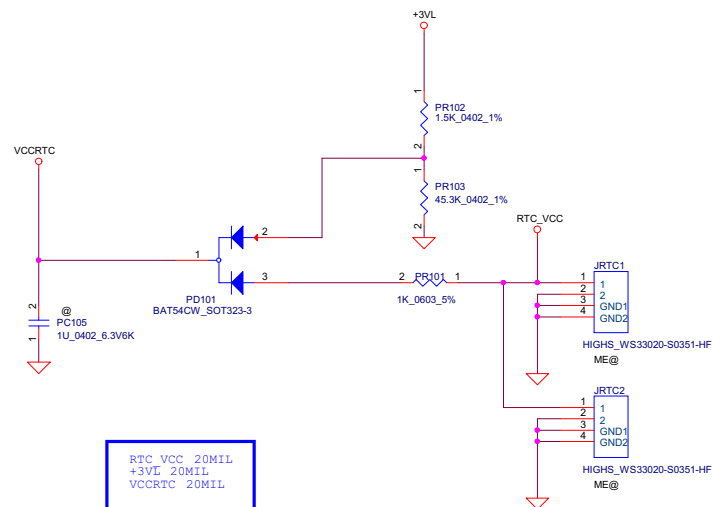
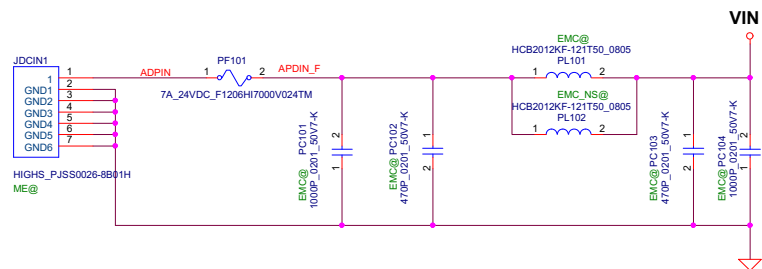
VDDQ_PGOOD

NA

DGPU_PWROK

CPU_VR_READY

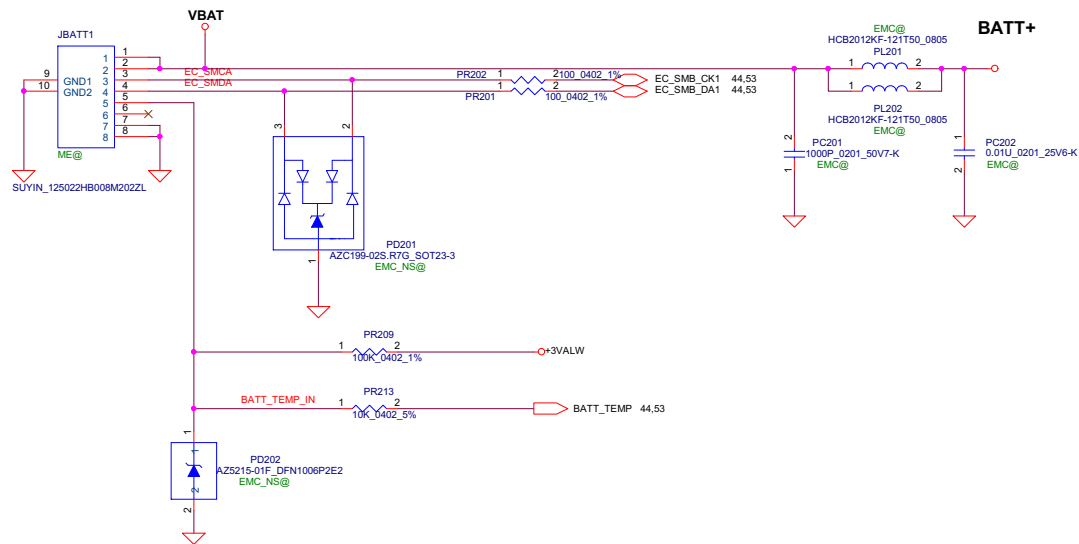
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-Power Diagram	
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				Customer	DG421
				Date	Sunday, January 25, 2017
				Sheet	50 of 60
				Rev	1.0



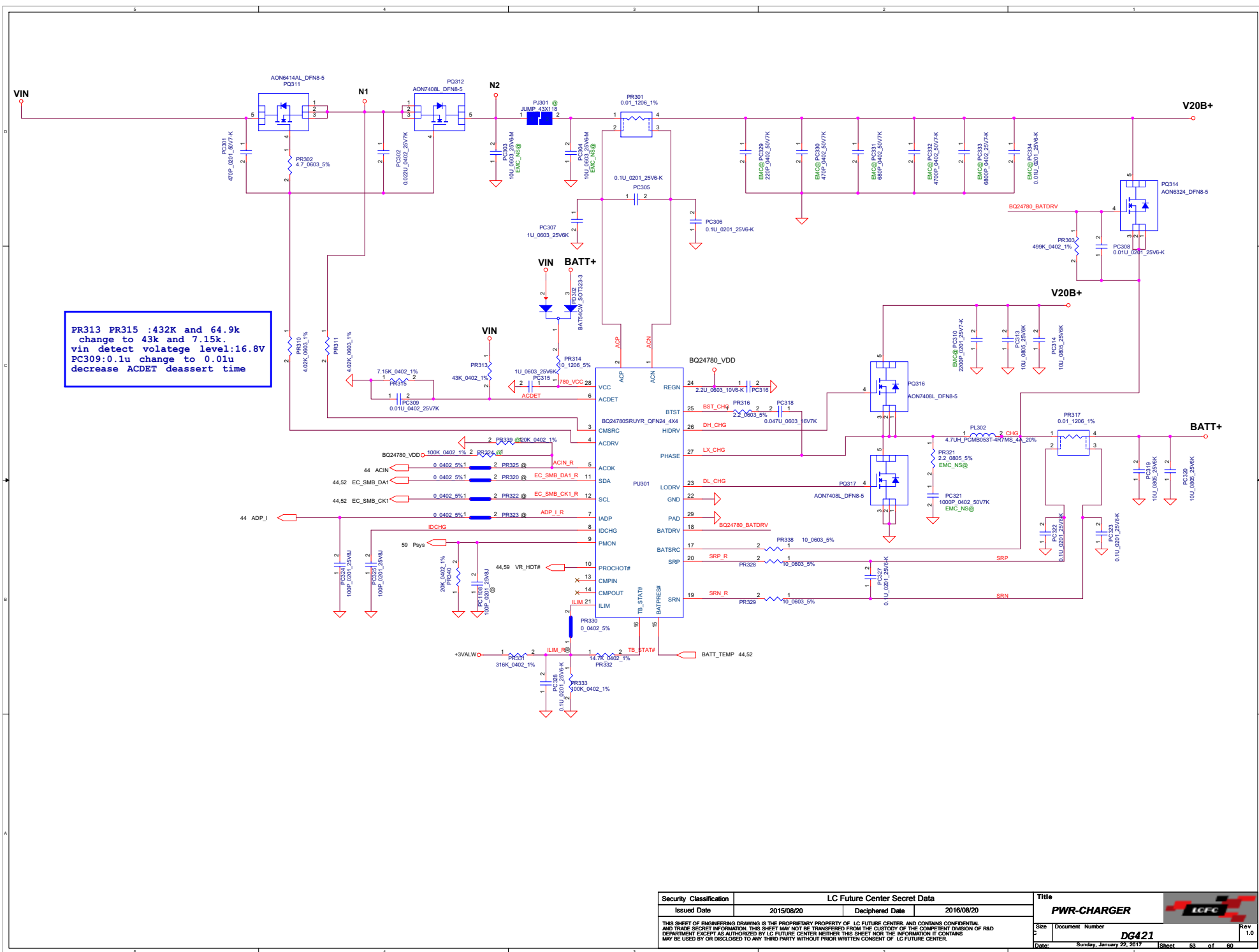
RTC VCC 20MIL
+3V_L 20MIL
VCCRTC 20MIL


No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)

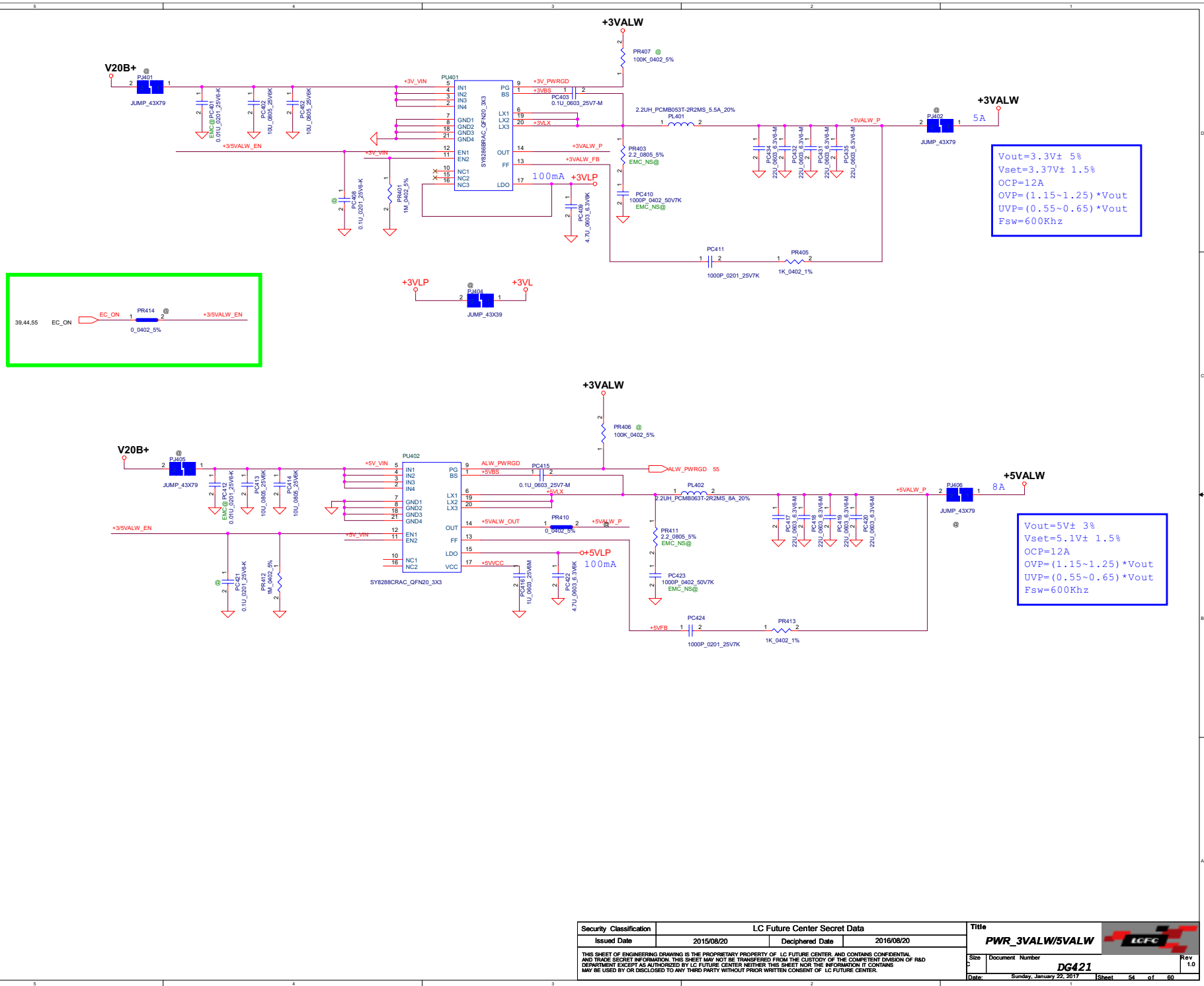
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-DCIN / RTC charger	
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2S1P polymer battery
voltage level: +6V ~
8.4 V



Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		PWR-CHARGER			
2015/08/20		2016/08/20		dg421		Rev 1.0	
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Date		Sunday, January 22, 2017		Sheet		63 of 60	



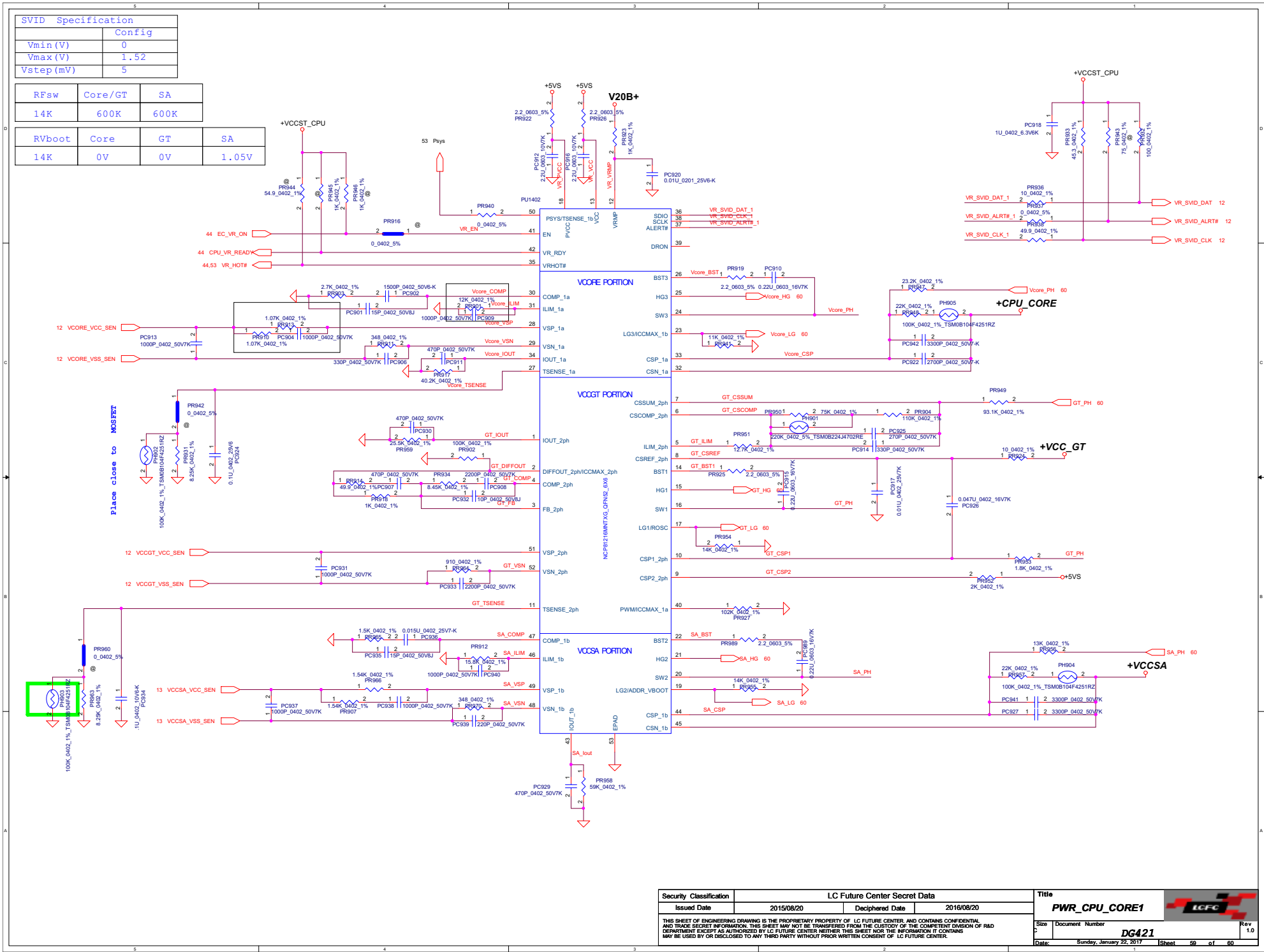
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR_3VALW/5VALW	
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Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR	
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				Document Number DG421	Rev 1.0
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SVID Specification	
Config	
Vmin (V)	0
Vmax (V)	1.52
Vstep (mV)	5

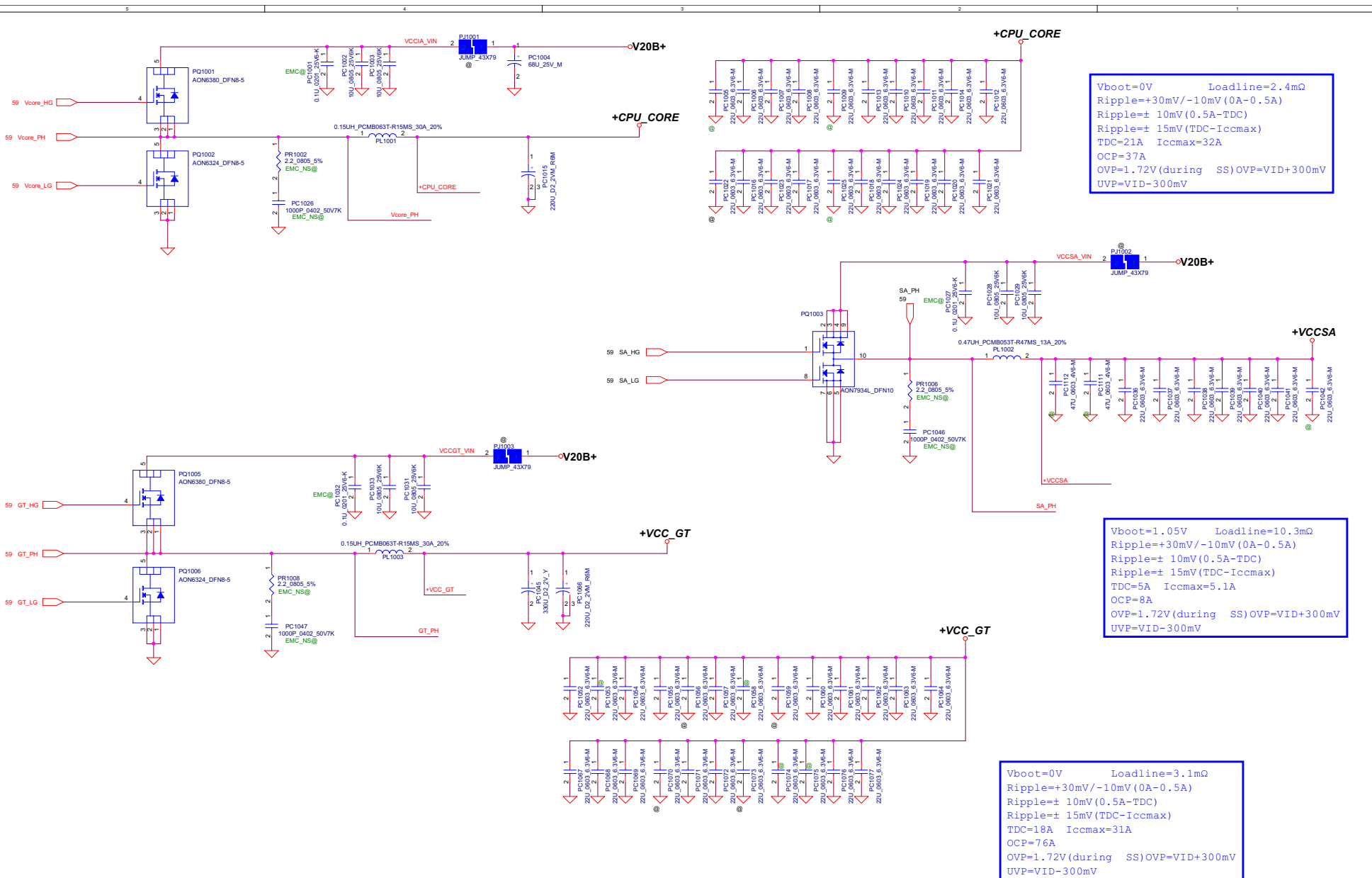
RFsw	Core/GT	SA
14K	600K	600K


RVboot	Core	GT	SA
14K	0V	0V	1.05V



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Issued Date	2015/08/20	Deciphered Date	2016/08/20
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Title		PWR_CPU_CORE1	
Size	Document Number	Rev	1.0
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		PWR_CPU_CORE2	
2015/08/20		2016/08/20			
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Size	Document Number		Rev		
	DG421		1.0		
Date	Sunday, January 22, 2017		Sheet	60	of 60